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VOICE OF THE ENGINEER

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H8SX

H8SX – 32-bit CISC, Single cycle, Powerhouse

Up to 1MIPs/MHz, fast multipliers/dividers, zero wait state Flash

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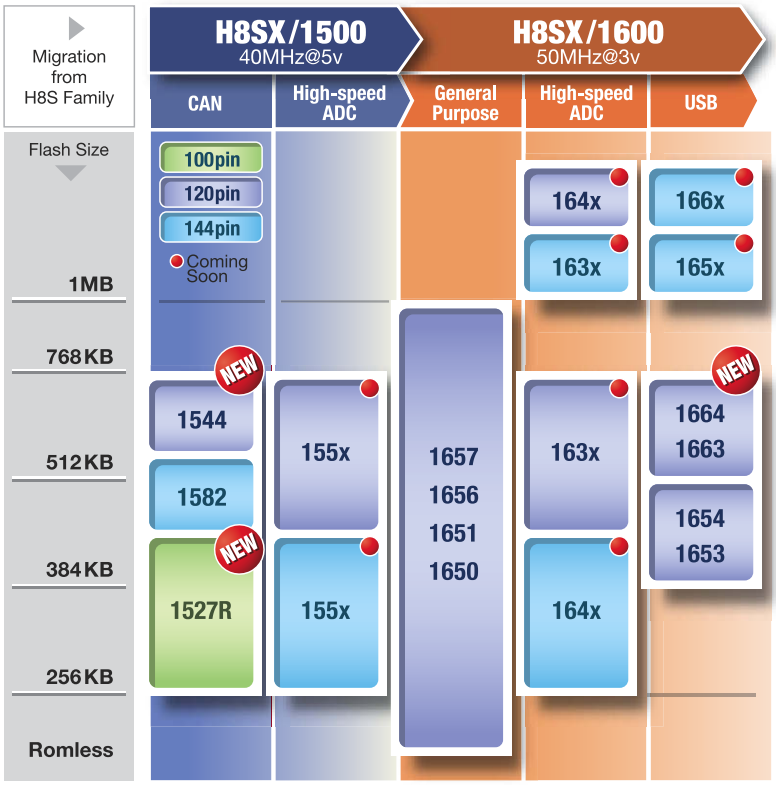
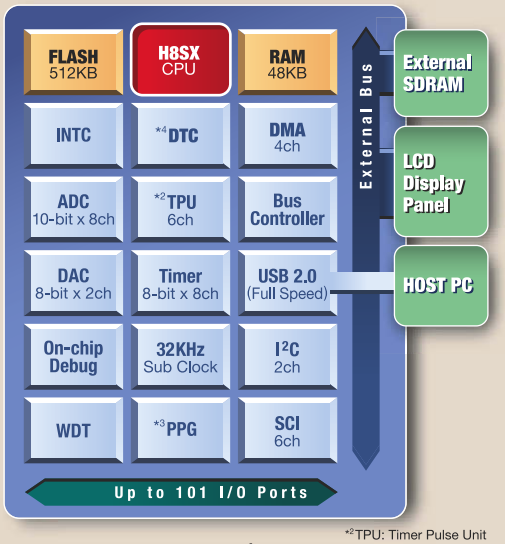
H8SX Product Roadmap



*1Source:Gartner Dataquest (April 2006) "2005 Worldwide Microcontroller Vendor Revenue" GJ06333

HOT Products | **H8SX/1664** | 50MHz@3v



*2TPU: Timer Pulse Unit
*3PPG: Programmable Pattern Generator
*4DTC: Data Transfer Controller

Top Reasons To Select H8SX

- **High-Performance**
  - 32-bit CPU with built-in hardware MAC. Up to 50MIPs
  - High-speed multipliers (single-cycle for 16-bit)
  - Majority of CISC instruction set executes in 1 cycle
  - Single-cycle access Flash (up to 1MB) and SRAM (up to 64KB) at maximum clock frequency
  - Multiple DMA engines and 3 bus architecture system, providing efficient data path management.
- **Compatibility**
  - Pin compatibility within H8SX families
  - Code and peripheral compatibility with H8S devices.
- **Connectivity**
  - Certified USB 2.0 Full Speed, Bus powered or Self powered
  - Six serial ports, Including IrDA and ISO7816. Two additional I²C interfaces
  - High-speed serial (921Kbps UART, 5Mbps Synchronous).
- **Timers**
  - Up to 12 channels of 16-bit timers with a total of 32 input capture/output compare
  - 20ns resolution

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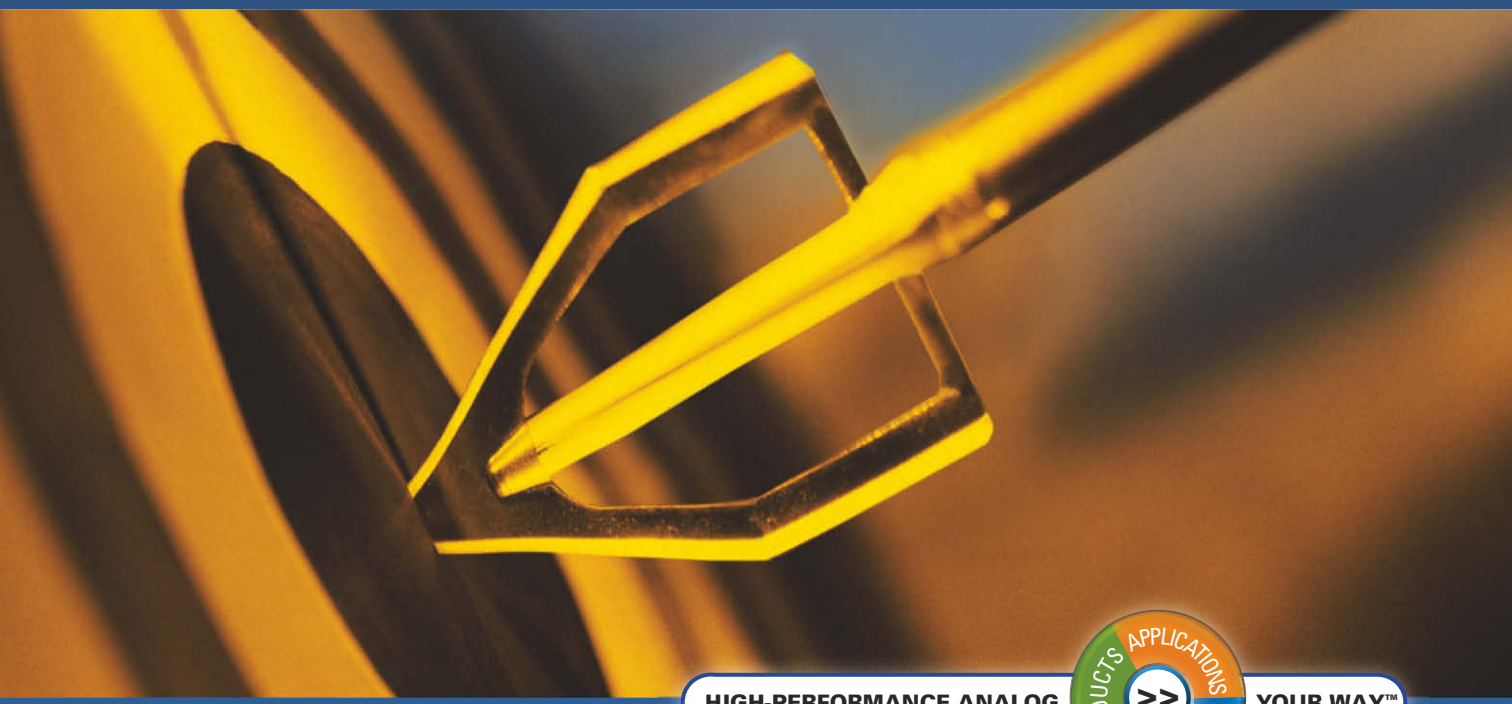

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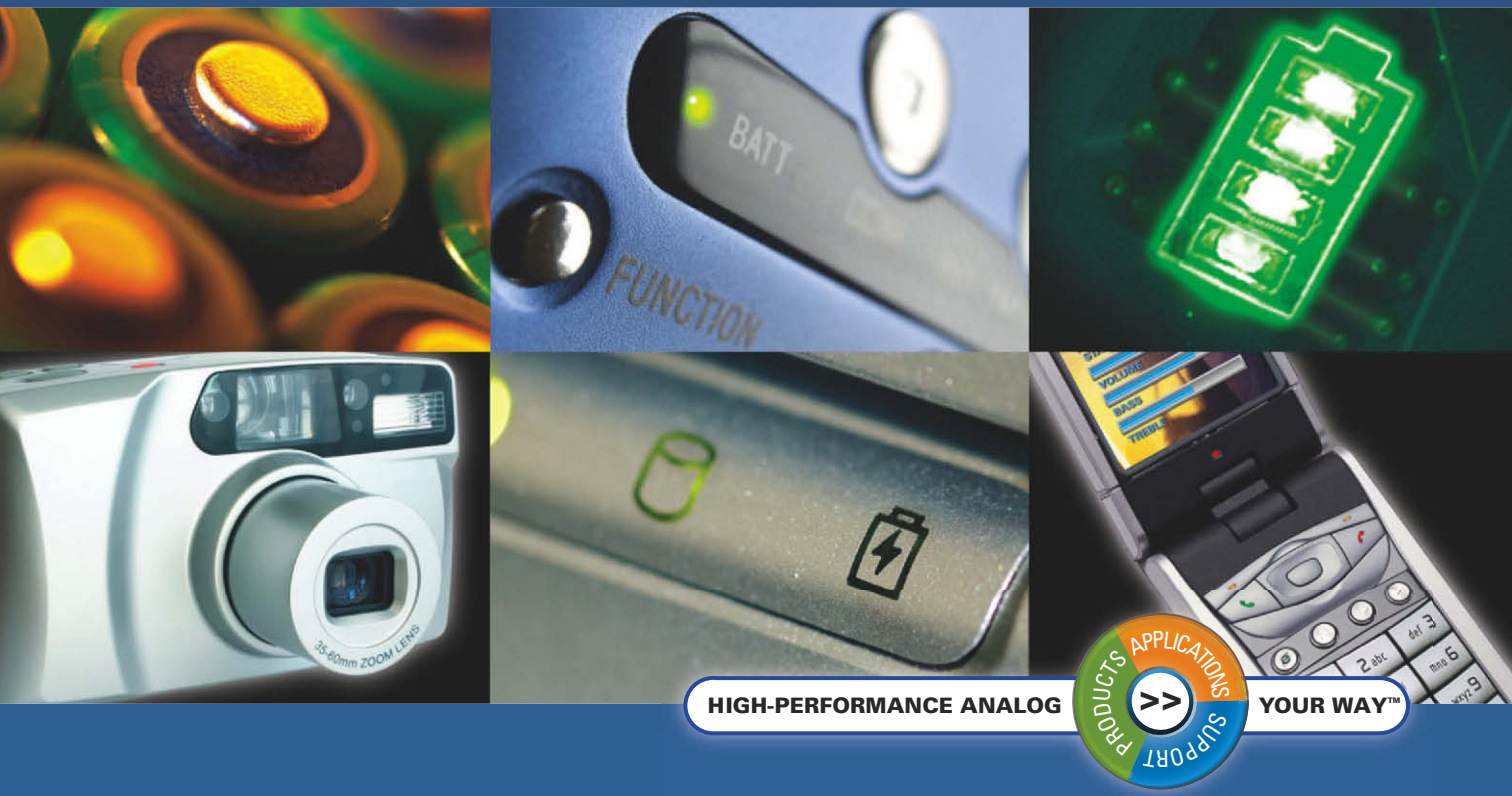

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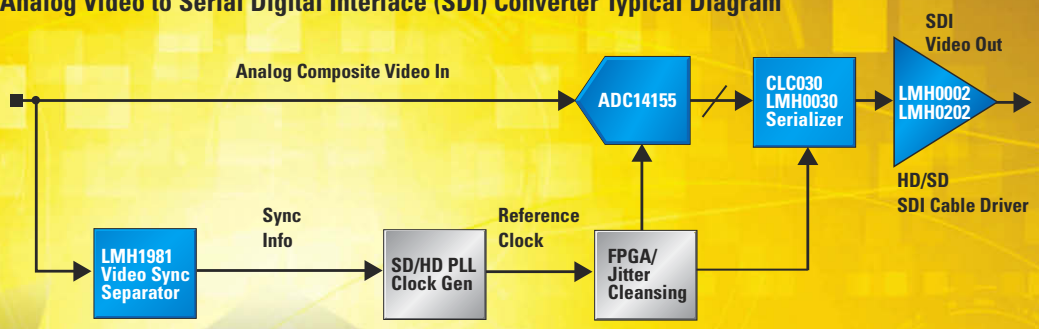
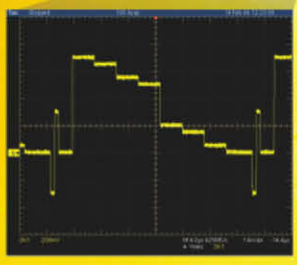
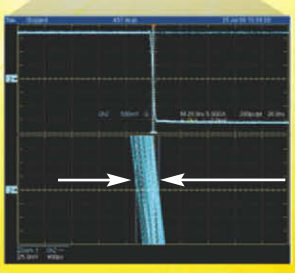
New LMH1981 Features 50% Sync Slicing for Precise Output Timing

Analog Video to Serial Digital Interface (SDI) Converter Typical Diagram





720p/60 Tri-Level Input



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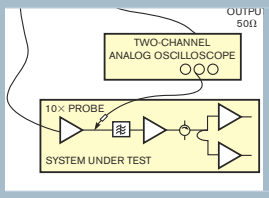

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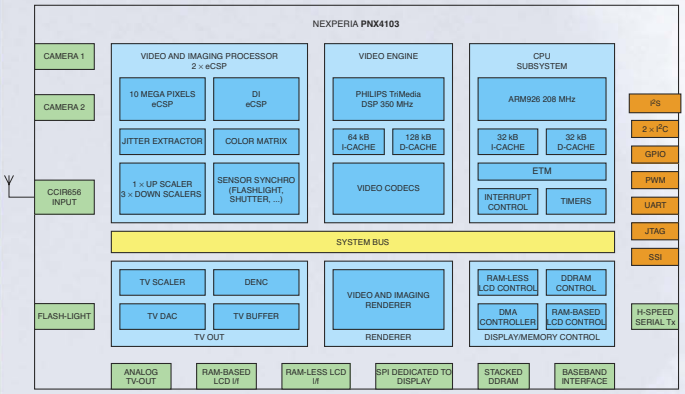

PNX4103, the advanced mobile multimedia processor

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What if you could

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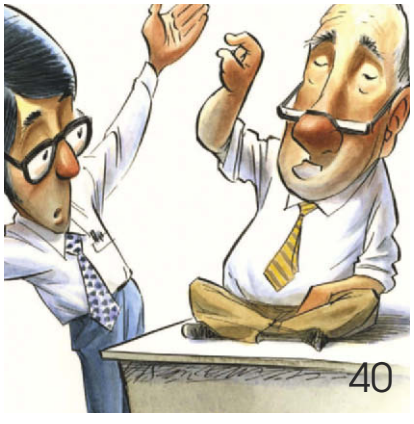

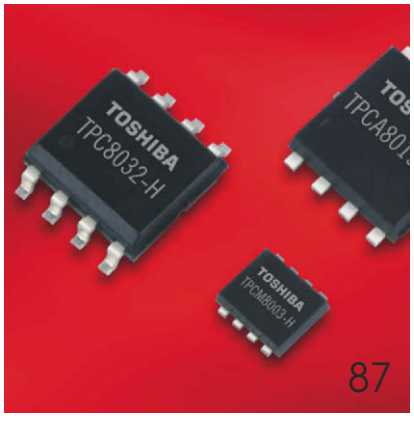

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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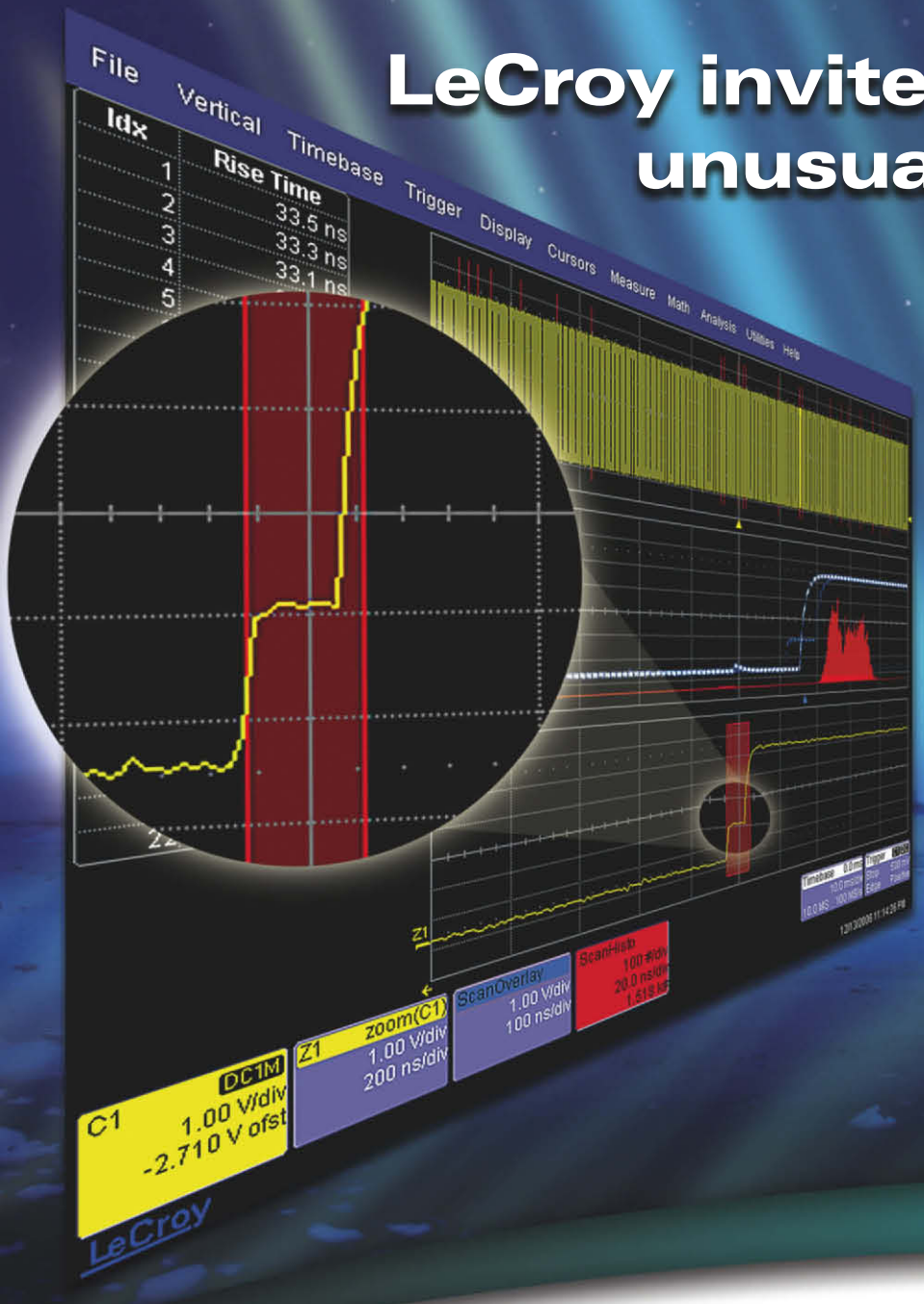

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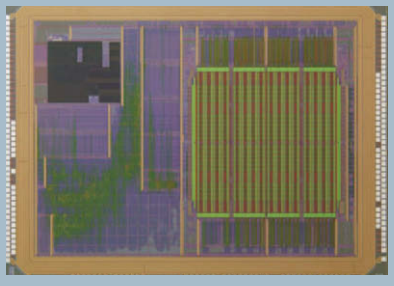

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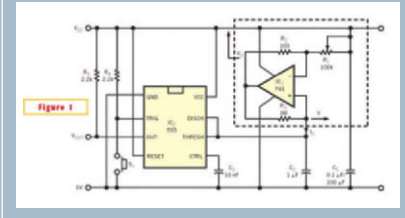

APRIL FOOLS' DAY

In recognition of April 1st, we offer the following Design Idea from 2003. Penned by now-deceased Design Ideas editor Bill Travis (we miss you, Bill), the article goes into a convincing amount of detail to describe a circuit that's capable of turning on a full 18 minutes before you press the button to activate it.
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BY BRIAN DIPERT, SENIOR TECHNICAL EDITOR

Consumer limitations

A recent editorial by *EDN* Editor in Chief Maury Wright claimed that "a more open approach to the Apple codec and DRM (digital-rights management) might ultimately serve the company much better than the current stance that limits content to Apple hardware" (**Reference 1**). Looking at my past write-ups, you might conclude that I'm in full agreement with my boss (**Reference 2** and **3**). Not so fast.

Although I'm generally an advocate of open standards, I also see plenty of examples in which a competing de facto standard thrives because it doesn't have to struggle with as much pace-slowing incompatibility or infighting between "partners" jockeying for proprietary "enhancements" or other means of market dominance.

One online comment on Wright's editorial, from Steve Gates, who identified himself as an engineer at Microsoft, struck me. Gates writes, "The current mishmash of products and technology from various 'partnerships' is the key reason digital devices have not proliferated at a much faster pace." He has a good point. I've encountered plenty of situations in which the setup simplicity of an Apple-like single-company ecosystem would have been a preferable, albeit perhaps more costly, alternative to the frustrating, more "open" alternative with which I was grappling.

For example, when friends recently expressed interest in Yahoo Music Unlimited's Microsoft codec- and DRM-based subscription service and in piping that music from their PC to their living room, I thought I'd let them do some hands-on testing of the WMB (Wireless Music Bridge) that Linksys, which publicly partnered with Yahoo on the WMB, had recently sent me for review.

The PC-based software for the WMB redirects audio that would otherwise go out the speakers or headphone jack, sending it instead out the computer's network port to a LAN-connected piece of hardware that subsequently feeds a stereo system's line-input jacks. The Linksys device originally sold for $150, but it's currently available on Amazon for a little more than $80. To hit that price and still turn a profit, Linksys' engineers had to cut a few corners. To wit, my friends didn't want to run CAT5 cable from their office to the living room, preferring to use the device's built-in Wi-Fi transceiver. However, because the WMB offers no integrated display or front-panel controls, they had to jump through a bewildering of hoops.

Two WMBs, five calls to technical support, and several weeks later, my friends gave up. They finally got the PC and WMB to "see" each other, but they could never achieve stutter-free audio playback. I point probable blame at the audio-rerouting PC-software stack, but who knows for sure?

Conversely, my friends were up and running *within an hour* of opening the box of the Roku SoundBridge M1000. At around $200, it's about twice the price of the WMB, but it includes both front-panel controls and an LCD. It prompts you to enter wireless-network parameters without any required PC intercession, and, as long as you have Windows Media Connect running on the PC, it'll find, organize, and play back the audio files stored on that PC.

The M1000 was straightforward, but the Apple alternatives are even more so. Check out Apple's equivalent to the WMB, the AirPort Express. Better yet, check out the video-inclusive AppleTV, which should be shipping by the time you read this. Computers and LAN clients automatically find each other using the Bonjour protocol. Apple has built support for those LAN clients into both the Mac OS and iTunes. Everything just *works*—maybe not in *all* cases, as a visit to Apple's support forums points out, but, I'd wager, a higher percentage of situations than what I've previously described. See why Microsoft's supplemented—or, if you prefer, supplanted—PlaysForSure with the Apple-reminiscent Zune strategy?

Ecosystem standards work only if ... well ... they *work*. Most customers don't understand technology, and you should not expect them to become IT experts to use your gear. Spend a few bucks more up-front on your system's bill-of-materials cost and, yes, your marketing counterparts will have to figure out how to sell a more expensive widget. But in exchange, you'll get fewer support calls and fewer product returns, both of which gobble up any profit margin you might have otherwise achieved with the up-front sale. Happier customers become *long-term* customers and convert others into customers. I'm with Steve Gates on this one. EDN

Contact me at bdipert@edn.com.

REFERENCES

For this EDN.comment's associated references, see the Web version: www.edn.com/070329ed.

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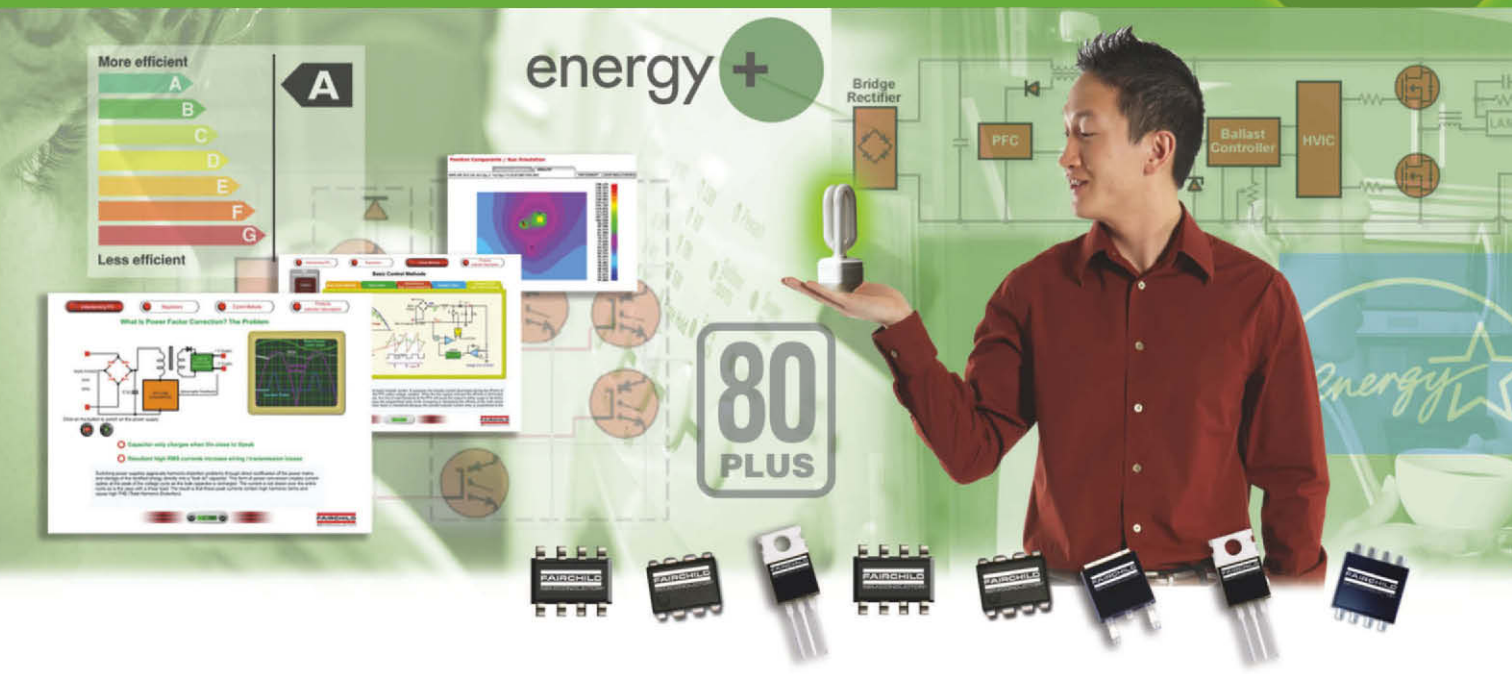

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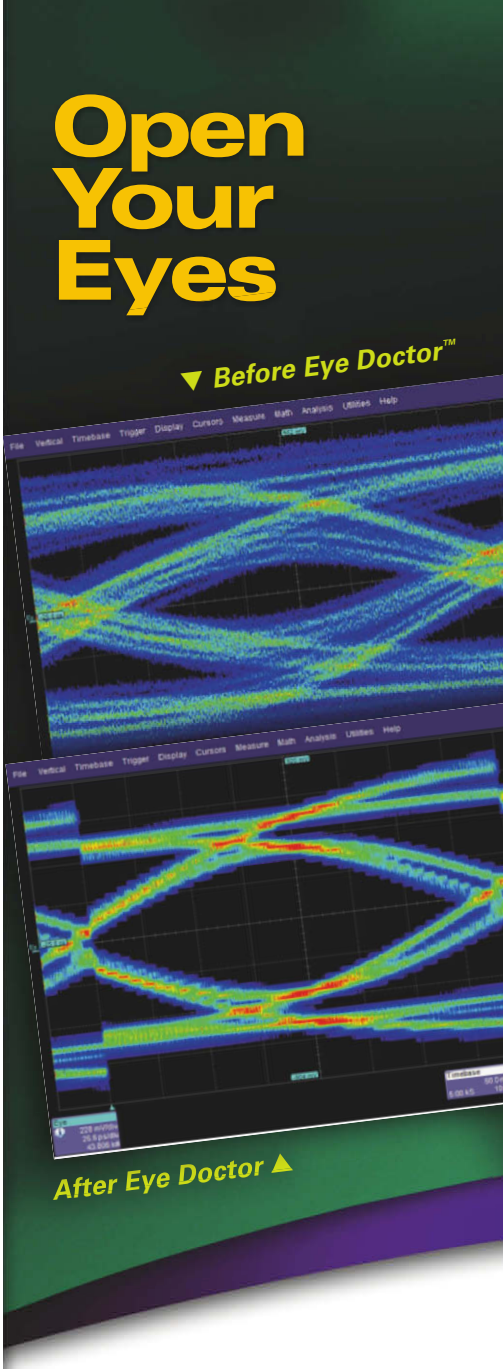

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RAQ's

Rarely Asked Questions

Strange but true stories from the call logs of Analog Devices

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Observing Maximum Ratings or How to Avoid Forecasts of Doom.

Q. How much safety margin is there in "absolute maximum" ratings?

A. None! And integrated circuits (ICs) are not fortune tellers.

An IC's absolute maximum rating is the limit of the conditions under which it may be operated. Operation beyond these limits will damage it, and may destroy it.

How far beyond the limits is never stated. Some devices are very robust, some are not, but no manufacturer will provide support for deviation from the limits. The only safe rule is to treat "never" as never. But understanding why exceeding absolute maximum limits can cause damage allows us to design better systems.

A zener diode is designed to conduct with a reverse voltage larger than its breakdown voltage and can safely carry large reverse currents. But other IC diodes, especially base-emitter junctions, are damaged by very small reverse currents, sometimes within a few microseconds. Similarly, the gate oxide of a MOS device broken down by an over-voltage is irreparably damaged. So, exceeding absolute maximum voltages may damage ICs by breaking down a junction or gate oxide.

Some absolute maximum voltages are expressed in terms of other voltages. In other words, the input voltage (V_{IN}) of an amplifier may be limited to V_{SS}–0.3 V ≤ V_{IN} ≤ V_{DD}+0.3 V, or the negative supply limit may be defined in terms of the positive supply $-V_{SS} \le V_{DD}$. The first means that the input voltage may not go more than 300 mV outside the supplies, while the second means that the magnitude of the negative supply must never exceed that of the positive supply. This does not mean that if you will be using a +10 V V_{DD} the input may go to +8 V, or the V_{SS} to –8 V *before* V_{DD} is turned on. Although silicon chips are crystals, they are not crystal balls and absolutely cannot foretell the future[1]. Absolute maximum specifications of this type indicate that power and signal sequencing is important. Exceeding this type of limit may not cause device breakdown, but is likely to turn on parasitic devices in the IC substrate, which in turn can latch up, short-circuit the power supply, and destroy the device by overcurrent or overheating.

In addition to voltage limits, the absolute maximum specification may limit chip dissipation, currents at certain pins, and chip and package temperatures. Sometimes transient dissipation and current limits may be higher than steady-state ones, but it is very important to understand — and remain within—all the prescribed limits.

[1]*Asimov, A "The Endochronic Properties of Resublimated Thiotimoline" ASF March 1948 (http://en.wikipedia.org/wiki/Thiotimoline)*

To learn more about absolute maximum ratings, Go to: http://rbi.ims.ca/5383-101

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INNOVATIONS & INNOVATORS

AWGs target digital-RF testing, provide optional digital outputs

Tektronix has announced the 600M- and 1.2G-sample/sec AWG5000 Series of AWGs (arbitrary-waveform generators), which use the same platform as the recently introduced 20G-sample/sec AWG7000 Series. Depending on the model, one AWG5000 can generate four 14-bit-resolution analog signals or two such signals plus—optionally—28 digital signals for testing of baseband and IF (intermediate-frequency) circuits in mixed-signal devices. Tek calls the AWG5000 ideal for testing digital-RF technologies, including software-defined radio, radar, and fourth-generation wireless-communication systems.

"Digital RF," which refers to a new class of ICs that combines digital computing and traditional analog-RF technologies, is a major technical driver enabling new wireless applications. Digital-RF ICs' combination of digital- and analog-signal-processing technology—ADCs, DACs, and RF functions—presents unique testing requirements. The new generators offer high resolution, a variable sample rate, and looping/branching capabilities. These capabilities enable the generation of waveforms much deeper than the 16M-sample/channel waveform memory (32M samples optional) and enable engineers to use mathematically defined or oscilloscope-captured signals to efficiently test emerging digital-RF applications.

Each of the two analog-channel units in the 600M- and 1.2G-sample/sec AWG5000 Series of arbitrary-waveform generators can optionally include 28 digital outputs.

If the DUT (device under test) uses an analog interface between its baseband and RF sections, you need a signal generator that provides high vertical resolution and high SFDR (spurious-free dynamic range) on both its analog I/Q (in-phase/quadrature) carrier amplitude and IF outputs. If the interface is digital, the generator must provide parallel digital outputs to drive the DUT's IF section. To assist in debugging and verifying prototype baseband/RF interfaces, a generator with both analog and parallel digital-baseband-signal outputs is ideal for creating, replicating, and generating either textbook signals or distorted, real-life signals that include such imperfections as noise, jitter, and glitches.

The AWG5000 Series comprises four Windows XP-based models, each of which can run Windows-based software applications of your choice. Each unit has a 10.4-in. touchscreen LCD, and all provide 80-dB SFDR and two digital markers per analog channel. The four-channel models are well-suited to testing 4×4 MIMO (multiple-input/multiple-output) systems. US retail prices begin at $25,000.

—by Dan Strassberg

▷**Tektronix Inc**, www.tektronix.com.

FEEDBACK LOOP

"The ability to use big screens with a PC is an astoundingly obvious use, especially with customers increasingly getting movies via their PCs. So, expect to see either vendors adding the ports due to customer pressure or low-end Asian vendors making screens with these ports to capture the market, like they did with DVD players, forcing the other vendors to follow suit."

—Roger Norbert, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6413792. Add your comments.

Cyclone III stirs up new programmable-logic opportunities

In an effort to broaden opportunities for programmable logic to more complex and cost-sensitive high-volume applications that engineers would traditionally design with ASICs or ASSPs (application-specific standard parts), Altera Corp is looking beyond logic elements with its Cyclone III line and is pushing a package of high performance, low power, and low cost to markets such as consumer electronics, automotive, and industrial.

The low-cost, 65-nm Cyclone III FPGA line delivers 5000 to 120,000 logic elements, as much as 4 Mbits of embedded memory, and as many as 288 DSP multipliers at 260 MHz. It uses staggered I/O pads to reduce die size and board space. The first product, the EP3C5E144C8, debuted this month. At 20% lower cost per logic element than the previous Cyclone generation, the Cyclone III EP3C5E144C8 sells for $4 (500,000). The line carries as many as twice the logic elements and multipliers as the 90-nm Cyclone II line, targeting DSP-intensive applications, such as digital upconverters and downconverters, FEC (forward-error correction), and video encoding.

Altera manufactures the devices on 300-mm wafers using TSMC's (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) 65-nm, low-power process, marking a first for Altera. TSMC has fine-tuned the process to provide the lowest static- and dynamic-power consumption for applications in the portable- and consumer-product markets, such as DVRs, handsets, and portable media players. The Cyclone III FPGAs have as many as 120,000 logic elements and 0.5W static-power consumption, approximately half the power consumption of the Cyclone II family. "The combination of the functionality, the power consumption, and the cost allows Cyclone III to go into new applications for programmable logic," says Danny Biran, vice president of product and corporate marketing at Altera. "The key point here is that logic density, or the number of logic elements, no longer tells the whole story, which is something new in the FPGA industry."

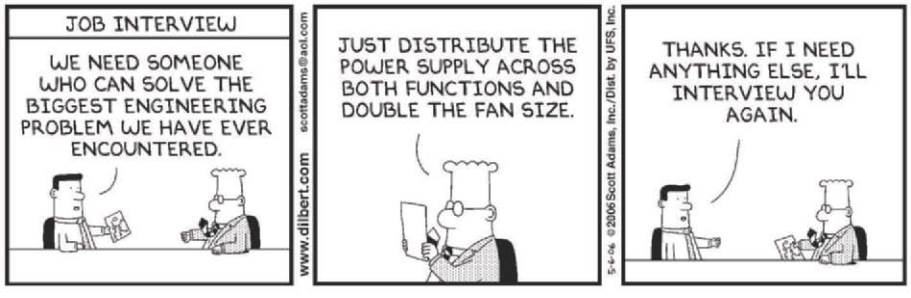
Altera is targeting software-defined radio, wireless base stations, video and image processing, and displays. The targets are especially smart, considering recent Gartner Dataquest (www.gartner.com) projections of a 15.9% CAGR (compound-annual-growth rate) for the overall programmable-logic-device market between 2004 and 2010, with automotive at a 49.7% CAGR and consumer at a 24.4% CAGR as the fastest growing segments. Altera is shipping the Cyclone III EP3C5E144C8 now to more than 250 customers, and production devices are scheduled to be available starting in August 2007. Altera has named Aldec, Altium, Magma, Mentor Graphics, and Synplicity (www.aldec.com, www.altium.com, www.magma-da.com, www.mentor.com, www.synplicity.com) as EDA partners. Altera expects to be shipping all eight members of the Cyclone III family by the end of 2007; the company's free Web edition of its Quartus II design software will support the devices.

> "Logic density no longer tells the whole story, which is something new in the FPGA industry."

—by Suzanne Deffree, *Electronic News*

▷**Altera**, www.altera.com.

DILBERT By Scott Adams



SOFTWARE CUTS TEST-LAB COMPUTER-CONFIGURATION TIME

03.29.07

EdenTree Technologies has announced Configuration Manager, a software tool that, according to the company, automatically reconfigures computers to radically reduce the time required for testing cycles in test labs. The package allows engineers to set up, archive, and restore Unix, Windows, and Linux computer systems in a fraction of the time that other approaches require.

Using manual methods, rebuilding or updating a computer with an operating system and applications can take hours or days. Through automation, Configuration Manager cuts that time to approximately 15 minutes. The product meets the needs of test labs that require systems under test and deployed systems to be configured identically. Configuration Manager, which sells for $1000 to $5000 per server depending upon server capacity, runs under Sun Solaris, Linux, and Windows operating systems.

—by Dan Strassberg

▶**EdenTree Technologies, www.edentreetech.com.**

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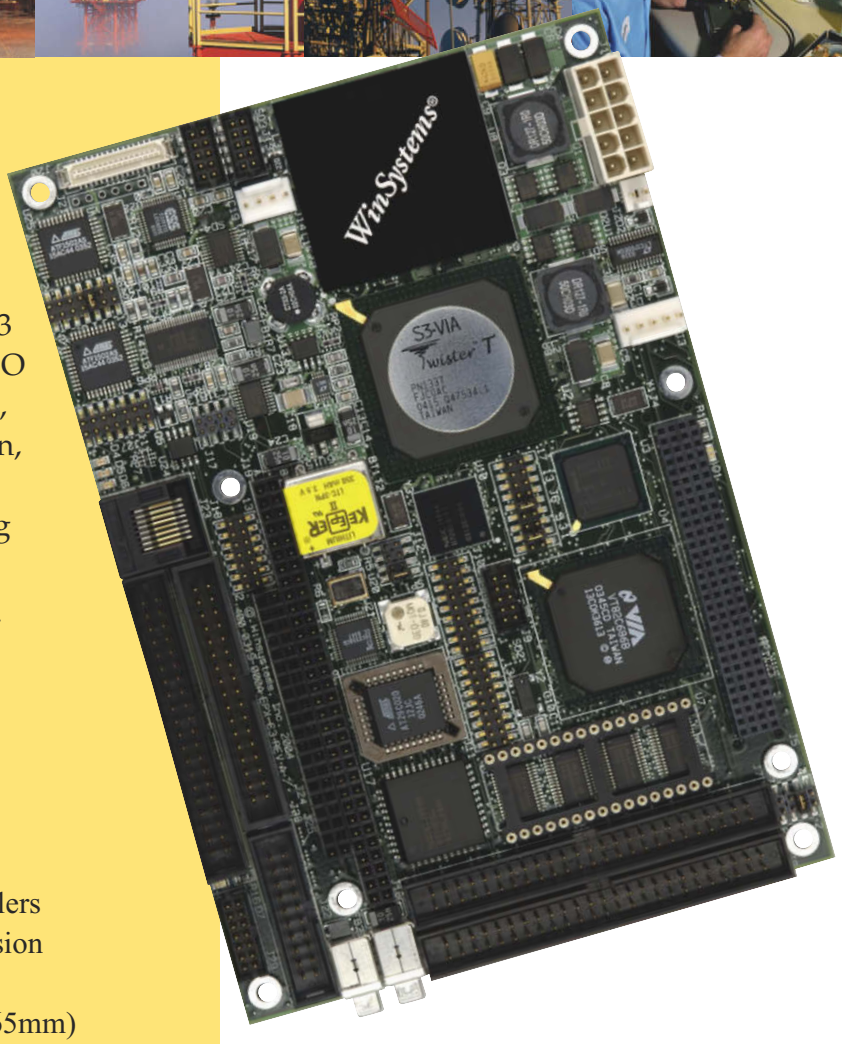

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Silicon foundations simplify assembly lines

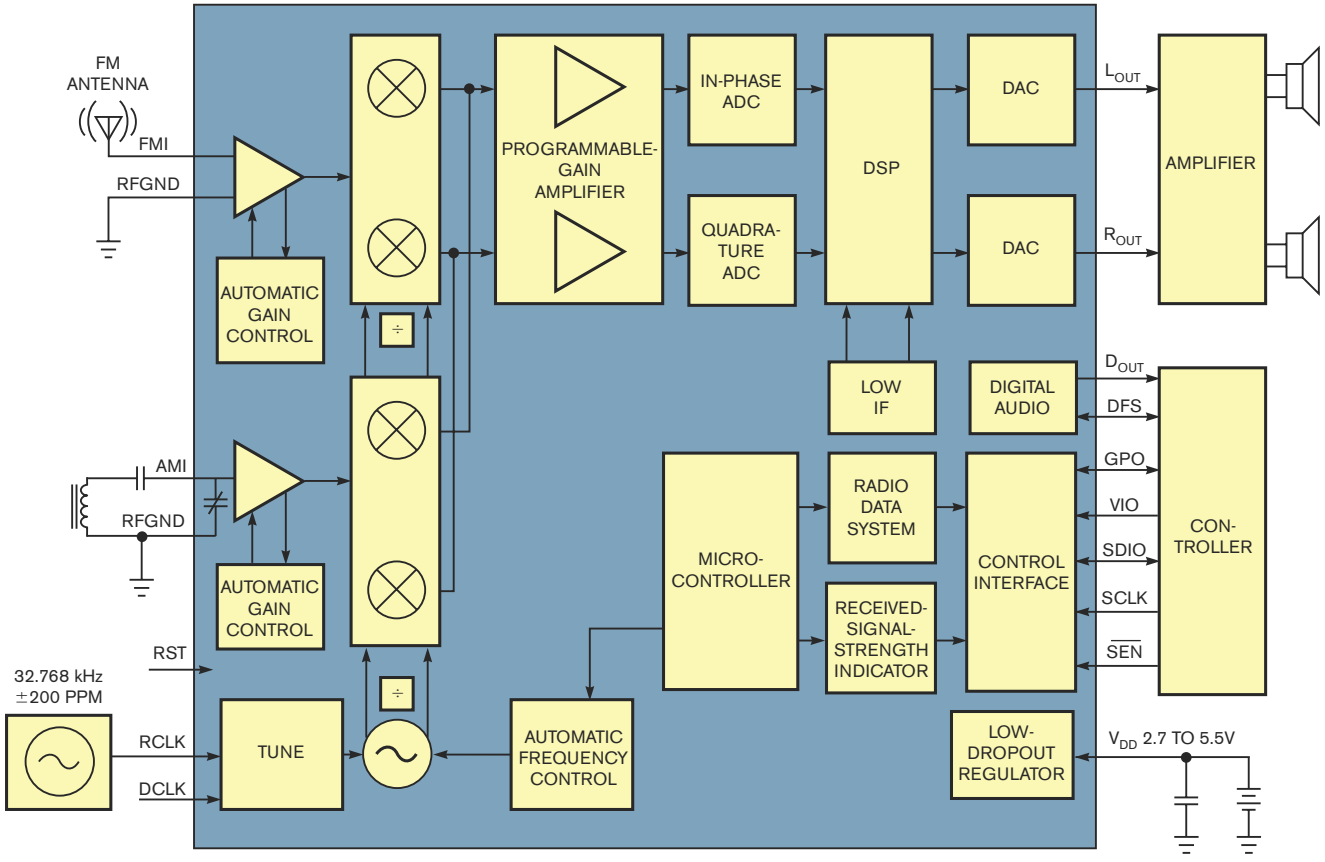
Two consecutive press briefings at January's Consumer Electronics Show dealt with different products for different markets but delivered a similar message: that by migrating from a traditional approach comprising numerous discrete components to an integrated one based on silicon building blocks, you can not only potentially improve your end-system specifications, but also dramatically simplify, boost the yield, and reduce the cost of your system-manufacturing flow.

In the first briefing, Xceive unveiled its XC5000 broadcast receiver for NTSC (National Television System Committee), ATSC (Advanced Television Systems Committee), QAM (quadrature-amplitude-modulated) digital cable, DMB-TH (digital-multimedia broadcast-terrestrial/handheld), DVB-C (digital-video broadcast-cable), DVB-T (digital-video broadcast-terrestial), and ISDB (Integrated Services Digital Broadcasting). Although the company fabricates this $6 (100,000-per-month) device on a nonstandard silicon-germanium BiCMOS process, Xceive has to date elected to go this route so that its products will deliver reception performance equal to or better than a traditional can tuner. Other notable specifications for the XC5000 include 5-msec-per-channel signal detection and package dimensions of 7×7×0.85 mm.

(continued on pg 24)

TABLE–XC5000 VERSUS TRADITIONAL CAN TUNER

	XC5000		Can tuner	
Noise figure (dB)	Less than 6	Better sensitivity	Approximately 8	European, Japanese CAN
Phase noise (dBc)	Less than −97 at 10 kHz, less than −106 at 100 kHz, less than −118 at 1 MHz	Low error rate at high symbol rate	Less than −85 at 10 kHz	TDA6650/1 in hybrid mode
SNR (dB)	Greater than 53	Noise free, clear analog picture	Approximately 48	Typical European, Japanese CAN



Silicon Labs' highly integrated Si4730 and Si4731 are significantly more svelte than a traditional AM/FM-receiver-subsystem design.

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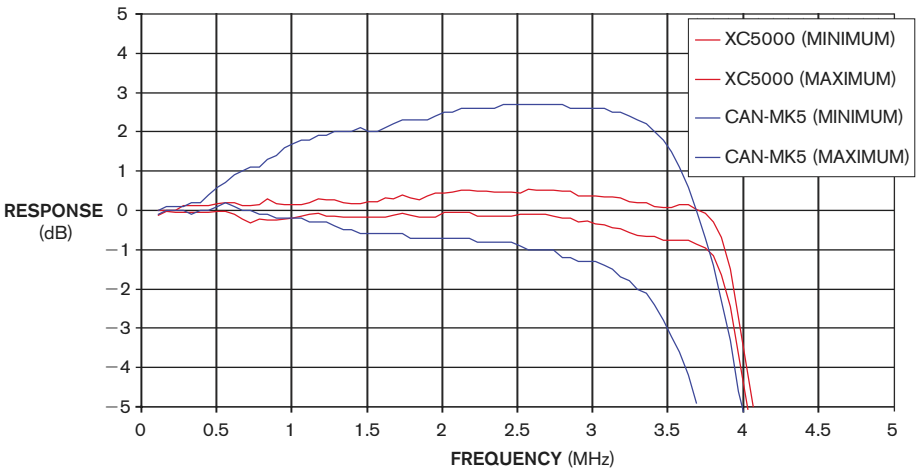

Xceive's XC5000 silicon foundation translates to decreased unit-to-unit SNR variability versus a traditional can television-broadcast receiver.

(continued from pg 22)

(Stack that up against a bulky can alternative!)

Because the XC5000 is software-configurable to support a wide range of worldwide broadcast parameters, it can single-handedly replace more than 30 geography-specific can-tuner configurations. (Xceive accomplished this task with one customer's television design.) The XC5000's silicon foundation also leads to decreased unit-to-unit SNR variability and superior frequency-response linearity versus can tuners. And, as conventional CMOS processes improve, Xceive will regularly revisit a course correction in that even-more-cost-effective-fabrication direction.

In the second briefing, Silicon Labs introduced its CMOS-based $4.87 (10,000) Si4730 and $5.53 (10,000) Si4731 AM/FM receivers; the 4731 also incorporates support for the European RDS (Radio Data System) and US RBDS (Radio Broadcast Data System), which enable display of data such as the station ID and song name. The devices' common 3×3-mm, 20-pin QFN (quad-flat-no-lead) package translates to an estimated 90+% less board area than a conventional discrete-assembled AM/FM receiver consumes, a particularly vital attribute in highly integrated, small-form-factor mobile-electronics devices, such as Microsoft's Zune. And some of the conventional receivers Silicon Labs showed were also assembly horror stories, comprising temperature- and age-sensitive components, such as hand-wound inductors and hand-tuned potentiometers. Conversely, the Si4730 and Si4731 are, like the earlier-described XC5000, software-configurable to support worldwide radio-broadcast parameters and capable of delivering consistently superior reception results.**—by Brian Dipert**

▷**Xceive**, www.xceive.com.
▷**Silicon Labs**, www.silabs.com.

ONESPIN SPINS EQUIVALENCE CHECKER FOR FPGA USERS

Formal-verification-tool maker OneSpin Solutions has made its 360 EC (equivalence checker) available to the FPGA market. The pushbutton 360 EC FPGA tool helps FPGA designers ensure that RTL (register-transfer-level) logic continues to operate properly when RTL undergoes synthesis to an FPGA netlist and when that netlist begins to operate in an FPGA architecture. The tool follows start-up OneSpin's first offerings, the OneSpin 360 MV (module-verifier) property checker and OneSpin EC ASIC, which debuted last year. The MV tool, which Infineon Technologies (www.infineon.com) developed and tested, targets IP (intellectual-property)-versus-RTL verification for ASIC and SOC (system-on-chip) designs, and the OneSpin EC ASIC primarily targets RTL-to-gates verification.

Wolfram Büttner, OneSpin's managing director and chief technology officer, says that 360 EC is the first commercial offering that effectively allows designers to check that a synthesis tool has correctly implemented a designer's creations–that is, that the synthesis is functionally equal to the design. OneSpin 360 EC FPGA is largely a pushbutton technology, which users run first after FPGA synthesis to ensure that the netlist functions according to the user's intent in RTL. Users can then ensure that the layout and netlist are functionally equivalent. For prototyping ASICs, users can check that the RTL for the FPGA is the same as the RTL for the ASIC. In all these use models, the tool flags areas that are not equivalent. In some cases, the tool highlights code or a section of the schematic in which it suspects errors have occurred; in other cases, the tool indicates approximately where an error occurs and pops up a waveform so that users can better pinpoint exact areas where mismatches occur.

The tool currently supports Synplicity (www.synplicity.com) and Altera (www.altera.com) Quartus II software environments and primarily targets high-end FPGAs, particularly those from Xilinx (www.xilinx.com) and Altera. Prices start at $137,500 for a one-year subscription. Many FPGA designers expect free or low-cost FPGA-programming tools, but the company's president and chief executive officer, Peter Feist, says that OneSpin 360 FPGA targets the 5% of FPGA users who are accustomed to ASIC-design flows and ASIC-tool prices.—by Michael Santarini

▶**OneSpin Solutions**, www.onespin.com.

03.29.07

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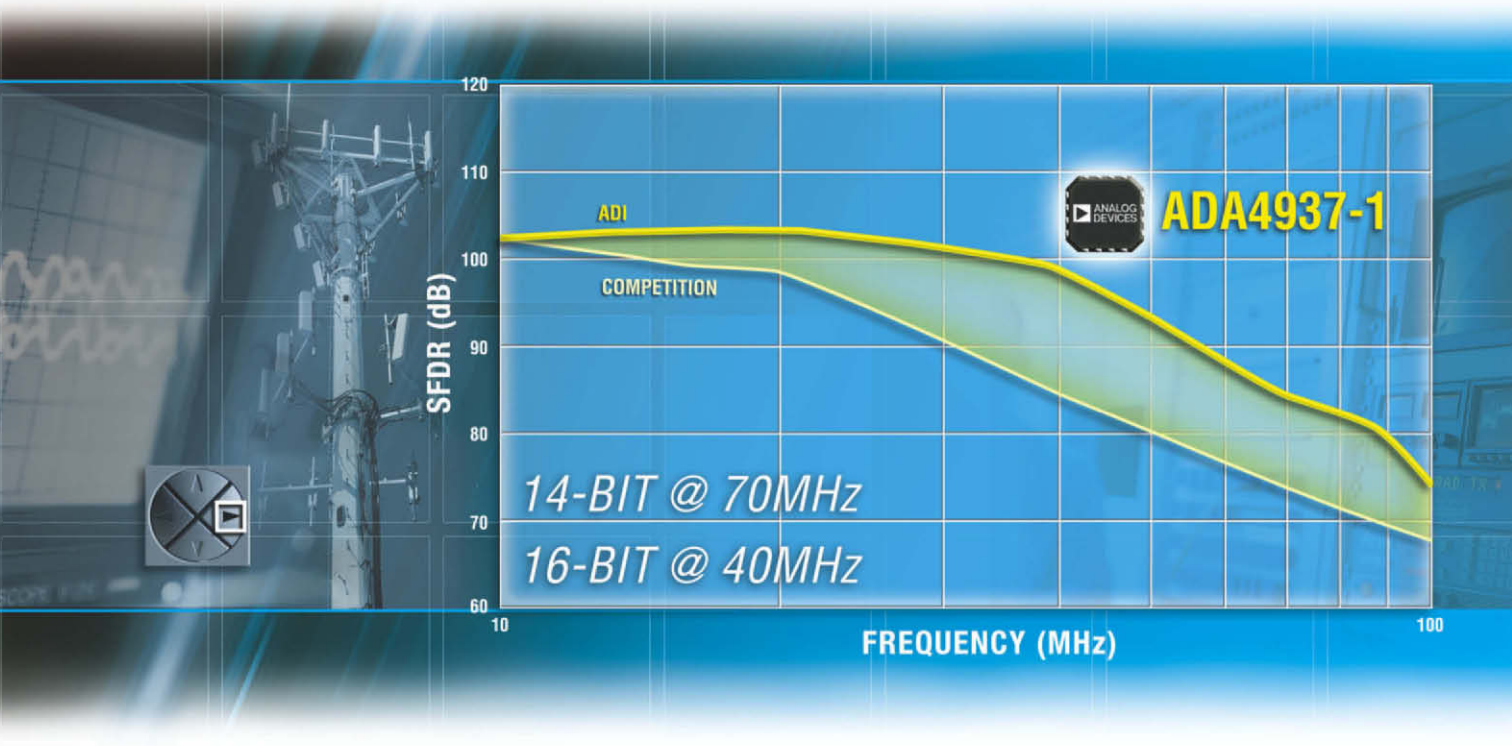

ADC	Bits	Channel Count	MSPS	Driver	
				ADA4937-1	ADA4938-1
AD9460/1	16	1	80/105/130		•
AD9446	16	1	80/100	•	•
AD9246/33	14/12	1	80/105/125		•
AD9245	14	1	20/40/65/80		•
AD9445	14	1	105/125	•	•
AD9254	14	1	150		•
AD6654	14	1	92.16	•	
AD9235/6	12	1	20/40/65/80		•
AD9230/11	12/10	1	170/210/250	•	
AD9215	10	1	65/80/105		•
AD9283	8	1	50/80/100		•
AD9480/1	8	1	250	•	
AD9640/27	14/12	2	80/105/125/150		•
AD9216	10	2	65/80/105		•
AD9288	8	2	40/80/100		•

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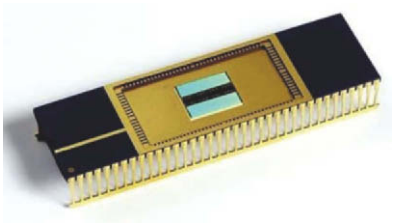
ANALOG DEVICES

RESEARCH UPDATE

BY RON WILSON



Samsung's phase-change memory sample comes in a small package targeting cell-phone-handset applications.

Phase-change memory creeps closer to the mainstream

Recent announcements by Intel and Samsung have made it clear that the companies, both of which have for years been pouring research funds into phase-change memory, are determined to bring the technology to market. Samsung was the first to move at the end of February, offering 256- and 512-Mbit engineering samples of its phase-change memory. The company built the device in 90-nm technology on 200-mm wafers and is aiming it to replace NOR-flash chips in cell-phone-handset applications, primarily because of the phase-change technology's much higher write speed.

Intel followed early this month with the announcement that it will offer a 128-Mbit, NOR-type device in 90-nm technology for sampling in the first half of 2007. The chip is a drop-in replacement for currently available NOR devices, but it will offer 100 million read-cycle endurance and greater-than-10-year data retention. Intel provides no speed figures.

▷**Samsung**, www.samsung.com.

▷**Intel**, www.intel.com.

FEEDBACK LOOP

"Long before the word 'hybrid' was in vogue, there were diesel-electric locomotives. ... They were hybrids in every sense of the word."

—A Robinson, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6402892. Add your comments.

ISM-band antenna measures less than 4 mm long

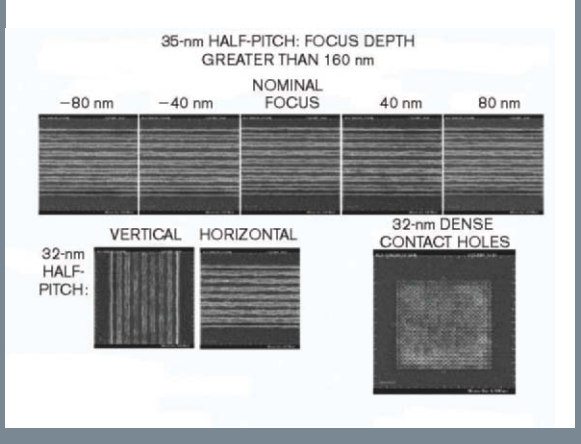
Fractus, a company that develops high-frequency antennas using area-filling-pattern technology, has announced development of an antenna measuring only 3.7×2 mm for the 2.4-GHz ISM (industrial/scientific/medical) band that Bluetooth, Wi-Fi, and ZigBee use. The antenna uses fractal geometry to produce patterns that optimally fill an area, allowing the antenna trace to occupy such a small space. The design has obvious advantages not only for mobile devices, but also for attachable or implantable radios in ID tags, medical devices, and the like, in which space is at a premium.

▷**Fractus**, www.fractus.com.

EUV-LITHOGRAPHY TOOL PRODUCES FIRST PATTERNS

03.29.07

ASML Optics has shown the first patterns using the full-field EUV (extreme-ultraviolet) alpha demo tool at the State University of New York–Albany's College of Nanoscale Science and Engineering (www.cnse.albany.edu). The tool is a prototype of what may become the successor to 193-nm optical lithography at or below the 32-nm-process node.



An EUV system prints 32-nm dense lines and contact-hole patterns (courtesy ASML).

The lithography system encloses an EUV, or "soft X-ray," light source; a complex set of mirrors; and a specially made mask in a large vacuum chamber to expose wafers. Because of the EUV's short wavelength, the system is theoretically capable of much greater resolution than is possible with 193-nm light, even after researchers play tricks with optics, illumination, multiple exposures, and OPC (optical-proximity correction).

The patterns include both groups of densely spaced lines at a 32-nm half-pitch and similarly dense arrays of contact holes at a 32-nm half-pitch. Researchers shifted the focus to show that they could achieve viable images with a depth of focus of more than 160 nm. They produced the mask with "little process optimization" and no OPC at all.

▶**ASML Optics**, www.asml.com.

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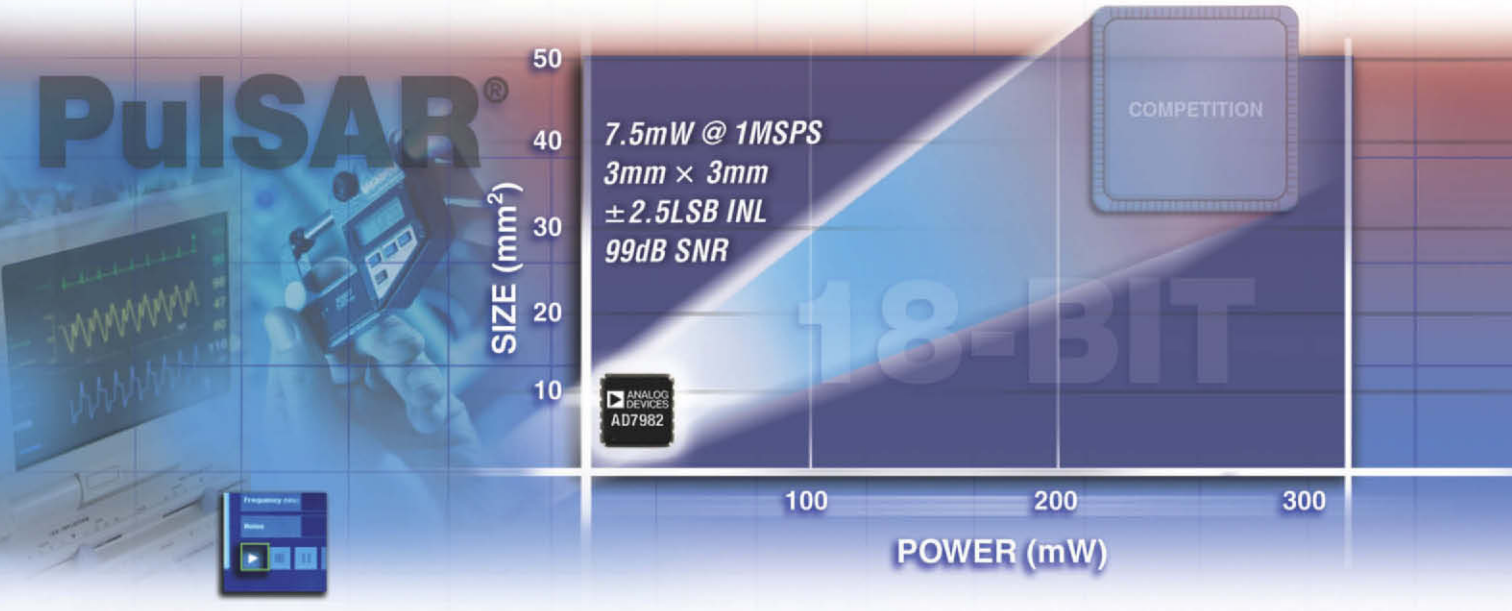

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AD7691	18	250 kSPS	±1.5 LSB, ±6 ppm	102 dB, 2.8 ppm	4.4 mW	14.50
AD7980	16	1 MSPS	±2 LSB, ±30 ppm	91.5 dB, 9.4 ppm	750 µW	19.50
AD7693	16	500 kSPS	±0.5 LSB, ±8 ppm	96.5 dB, 5.3 ppm	3.6 mW	18.00
AD7685	16	250 kSPS	±2.5 LSB, ±38 ppm	93.5 dB, 7.5 ppm	1.35 mW	6.50
AD7942	14	250 kSPS	±1 LSB, ±61 ppm	85 dB, 20 ppm	1.25 mW	4.75

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ANALOG DEVICES

BY HOWARD JOHNSON, PhD

Pulse-width compression

The signal in **Figure 1** originates in a pristine state at its transmitter. After passing through a long coaxial cable, high-frequency losses within the cable round off the signal edges, making each edge somewhat less steep at the receiver than at the transmitter.

Notice what happens at Point A. The received signal does not have time to fall completely down to the bottom before it must turn around and head back up. The positive-going step at Point B therefore begins life with a head start, as if sitting on a pedestal of height H.

The pedestal reduces the distance the signal must traverse to cross its threshold. The signal at Point B, because of the pedestal effect, crosses the receiver threshold early. The degree of advancement of edge B is a predictable function of the cable's attenuation characteristics. It happens the same way every time you repeat the experiment.

The received pulse after the data slicer (following the comparator, but before sampling) comes out narrower than you would expect due to the advancement of edge B. That pulse-narrowing effect is called *pulse-width compression*.

All bandwidth-limited systems built from conductive transverse-electromagnetic-mode transmission lines exhibit a similar effect. High-frequency losses always narrow a short pulse if that pulse is preceded by a long string of ones or zeros.

You can make the degree of pulse-width compression at the output of the data slicer into an excellent indicator of transmission-line performance.

This measure of performance interests me because I've noticed in recent years how difficult it has become to probe signals at the end of a high-speed serial link.

For one thing, the signal often enters a chip from underneath on BGA balls, providing no opportunity to attach a probe. Even if you could probe the signal from vias available on the back side of the PCB (printed-circuit board), those vias may not lie sufficiently close to the receiver to afford a good view of the received signal.

For example, in a 6.25-Gbps link, the signal rise/fall time at the receiver is on the order of 100 to 160 psec. Suppose that the input capacitance of the receiver creates a reflection equal to 20% of the received-signal amplitude. At the receiver location, that reflection appears coincident with each rising or falling edge, delaying each edge but possibly not affecting data reception. At a via just 0.25 in. away, that same reflection appears 90 psec later, assuming a round-trip delay of 0.5 in. at 180 psec/in. This additional round-trip delay places the 20% reflection at an apparent position near the center of the data eye. At that position, the reflection may appear formidable. To overcome this timing impediment, you must place your probe within a short fraction of one rise/fall time of the bitter end of the link. You must also select a probe that does not inordinately load down the signal under test—a requirement that is becoming increasingly difficult to meet.

Pulse-width compression works well as a measure of system bandwidth because it overcomes the limitations of probe placement and loading. It also measures the whole system up to and including the data slicer. EDN

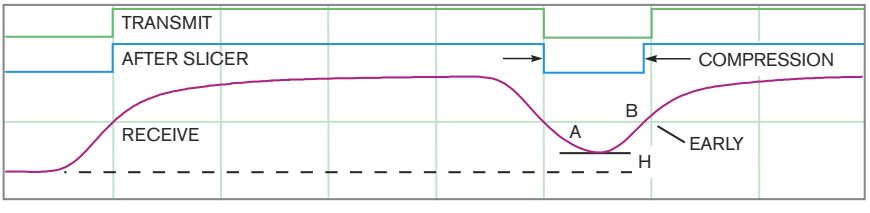

Figure 1 After receiving a long string of ones, the pulse-width-compression effect advances the positive transition at Point B.

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Howard Johnson discusses PCB-trace losses. See his video at www.edn.com/techclips. And stay tuned to this link for more videos to come.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com or e-mail him at howie03@sigcon.com.

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No. 117

Overcoming Challenges in Designing Step-Down Regulator Applications with ≥40V Input Voltage

— By Robert Bell, Applications Engineer

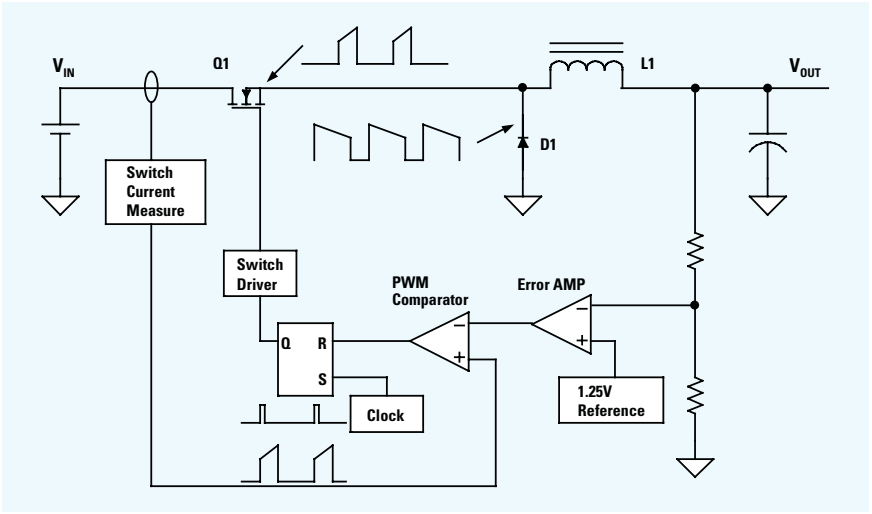

Figure 1. Buck Regulator Using Current Mode Control

Switching regulators are commonly used to step-down a higher level, unregulated input voltage to a regulated output voltage. In applications requiring DC-DC conversion from a relatively high input voltage, a switching regulator will dramatically improve conversion efficiency relative to linear regulator alternatives. Two of the most common transformer based DC-DC converter topologies are the Flyback and Forward. These topologies are very effective for high input to output step-down ratios since the transformer turns ratio can be set to accomplish the majority of the step-down conversion. For example, the conversion equation for a Forward converter is approximately: $V_{OUT} = V_{IN} \times D \times Ns/Np$

Where D is the duty cycle of the modulating switch, and Ns and Np are the quantities of the transformer secondary and primary turns. For V_{IN} = 66V

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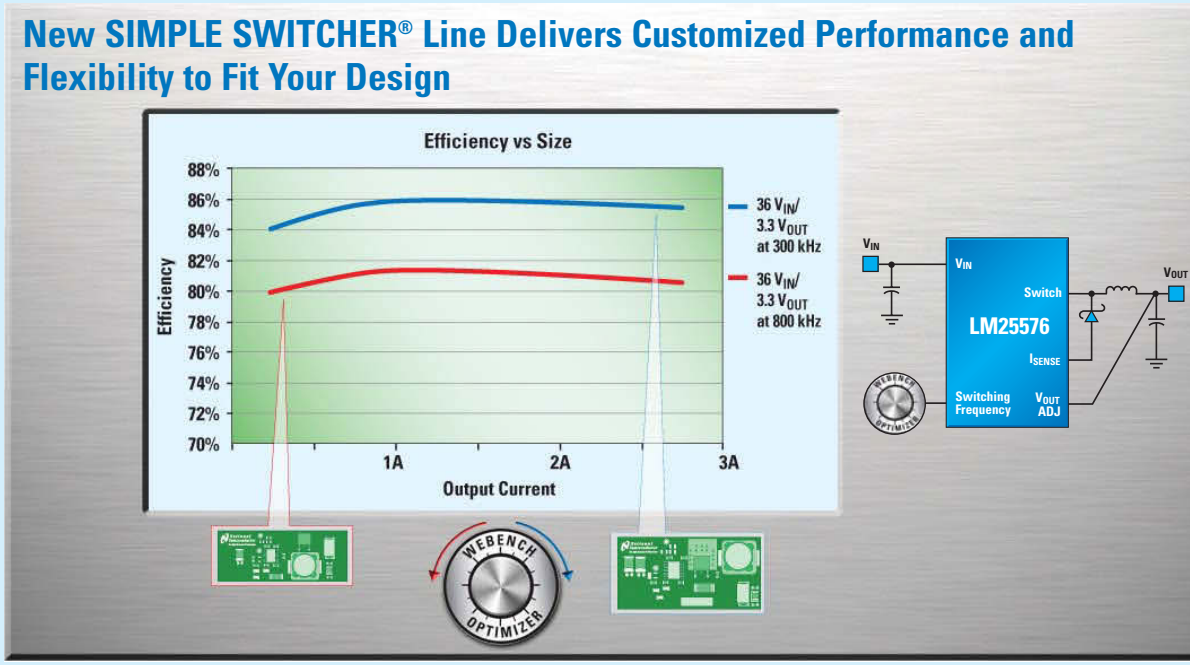

Product ID	Eval Board ID	V_{IN} Range (V)	V_{OUT} (V) Min	I_{OUT} (A)	f_{SWITCH} Range	Packaging
LM5576	LM5576EVAL	6 to 75	1.225	3	50 kHz to 500 kHz	TSSOP20-EP
LM25576	LM25576EVAL	6 to 42	1.225	3	50 kHz to 1 MHz	TSSOP20-EP
LM5575	LM5575EVAL	6 to 75	1.225	1.5	50 kHz to 500 kHz	TSSOP16-EP
LM25575	LM25575EVAL	6 to 42	1.225	1.5	50 kHz to 1 MHz	TSSOP16-EP
LM5574	LM5574EVAL	6 to 75	1.225	0.5	50 kHz to 500 kHz	TSSOP-16
LM25574	LM25574EVAL	6 to 42	1.225	0.5	50 kHz to 1 MHz	TSSOP-16

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Design Challenges In Step-Down Regulator Applications

and V_{OUT} = 3.3 (20:1 step down) the transformer turns ratio (Ns/Np) can be set to 1:10, requiring the modulation switch duty cycle to be 50%. For a 500 kHz operation, the 50% duty cycle equates to a switch on-time of 1 µs. For applications that do not require ground isolation, a Buck regulator is a more desirable topology. The buck topology provides a lower cost solution since it does not require a transformer. The conversion equation for a buck regulator is simply: $V_{OUT} = V_{IN} \times D$

Buck regulator applications with a high input to output step-down ratio require a small duty cycle. Coupled with high-frequency operation, the on-time for the modulating switch becomes very small. The high frequency and high step down ratio imposes significant challenges for the pulse-width modulation (PWM) controller. A buck regulator with V_{IN} = 66V and V_{OUT} = 3.3V operating at 500 kHz will require an on-time of 100 ns.

Common modulation control methods often used in buck regulators include Voltage Mode (VM), Current Mode (CM), and Constant On-Time (COT) control. Current-mode control provides ease of loop compensation and inherent line feed-forward compensation which make this method a favorite among power designers. Voltage-mode control is typically less noise sensitive but under-performs current mode in transient response and ease of stabilization. Constant On-Time control eliminates most of the stability-related issues and responds well to line and load transients. However, COT controlled regulators do not operate at constant switching frequency and cannot be synchronized to an external clock.

Figure 1 shows the block diagram of a buck regulator utilizing the current-mode control method. The output voltage is monitored and compared to a reference, with the resulting error signal applied to the PWM. The origin of the modulating ramp is where voltage mode and current mode control differ. The modulating ramp used in current mode control is a signal proportional to the buck switch current. The inductor current flows through the buck switch during the switch on-time. During this time, the inductor current waveform has a positive slope of $(V_{IN} - V_{OUT})/ L$. An accurate, fast measurement of the buck switch current is necessary to create the modulating ramp signal. The main disadvantage of current-mode control is the difficulties encountered creating the buck switch current signal.

Propagation delays and noise susceptibility make it almost impossible to use conventional current-mode control for high input voltage, large step-down buck regulator applications where very small on-times are required. Measuring the buck switch current is challenging. The measurement techniques commonly used are, make a voltage measurement across a shunt resistor or the buck switch 'on' resistance or use a current mirror circuit coupled to the buck switch. Each method requires a level shift to transpose the measured signal down to the ground reference for application to the PWM comparator. Even with the best design practices, current sense and level shift circuits will add a significant propagation delay. Another challenge is, when the buck switch is turned on, the free-wheel diode (D1) will turn off. A reverse recovery current will flow through the diode and the buck switch, causing a leading edge current spike and an extended ringing period. This spike can cause the PWM comparator to prematurely trip, causing erratic operation. The most common solution is to add filtering or leading edge blanking to the current sense signal. Attempts to filter or

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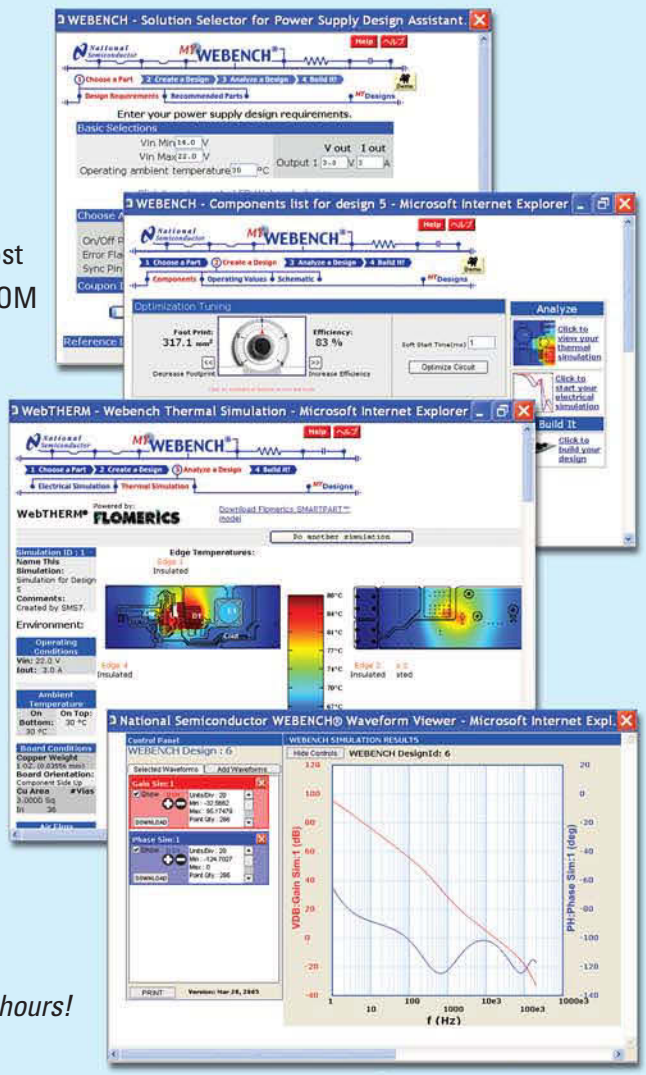

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Design Challenges In Step-Down Regulator Applications

blank this leading-edge spike increase the minimum controllable on-time of the buck switch.

Creating an Emulated Current Sense Signal

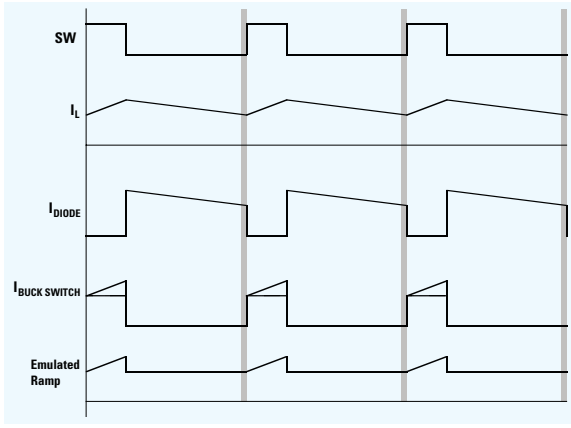

Figure 2. Buck Regulator Waveforms

The challenge of accurate and fast buck switch current measurement can be avoided with a new method that emulates the buck switch current without actually measuring the current. In a buck regulator, the inductor current is the sum of the buck switch current and free-wheel diode current, as shown in ***Figure 2.*** The buck switch current waveform can be broken down into two parts, a base or pedestal and a ramp. The pedestal represents the minimum inductor current value (or valley) over the switching cycle. The inductor current is at its minimum the instant the free-wheel diode turns off, as the buck switch turns on. The buck switch and the diode have the same minimum current value, occurring at the valley of the inductor current. A sample-and-hold measurement of the free-wheel diode current, sampled just prior to the turn-on of the buck switch can be used to capture the pedestal level information.

The other part of the buck switch current waveform is the ramp portion of the signal. The voltage across the inductor is the difference between the input (V_{IN}) and output (V_{OUT}) voltages when the buck switch is on. This voltage forces a positively ramping current through the inductor and the buck switch. The ramping current slope is equal to: $di/dt = (V_{IN} - V_{OUT}) / L$. An equivalent signal can be created with a voltage controlled current source and a capacitor. The rising voltage slope of a capacitor (C_{RAMP}) driven by a current source (I_{RAMP}) is equal to: $dv/dt = I_{RAMP} / C_{RAMP}$. If the current source is set proportional to the difference between the input and output voltages the capacitor ramp slope is equal to: $dv/dt = K \times (V_{IN} - V_{OUT}) / C_{RAMP}$, where K is a scale factor for the current source and C_{RAMP} is the ramp capacitor. The value of C_{RAMP} can be selected to set the capacitor voltage slope proportional to the inductor current slope.

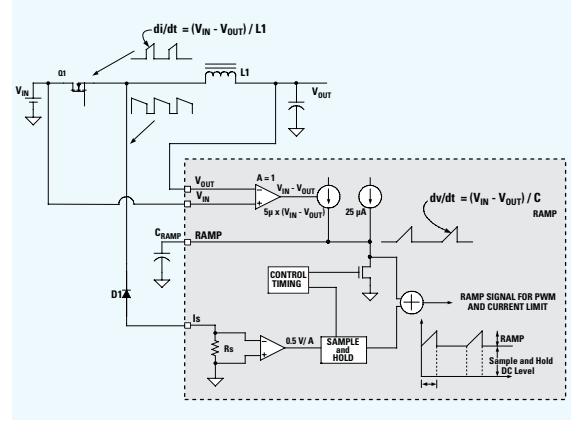

Figure 3. Emulated Current Mode Control Ramp Generator

Figure 3 presents the block diagram of the LM25576, one of six new integrated buck regulators that implement the emulated current mode control scheme described above. The top portion

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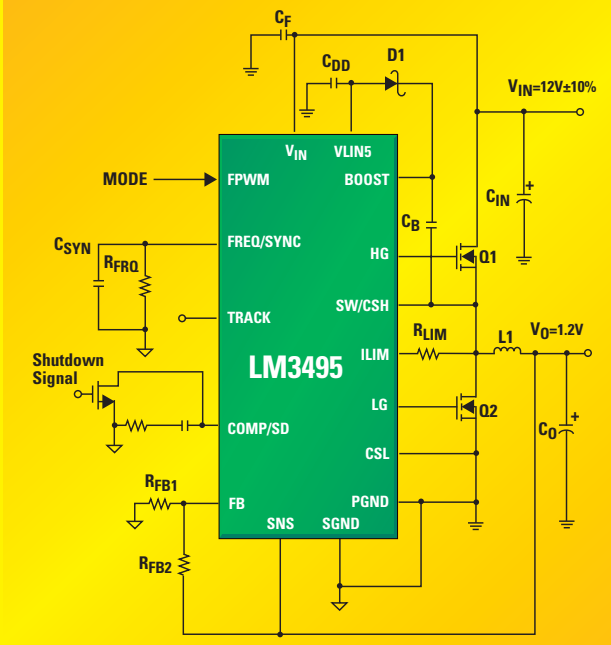
Typical Application Diagram



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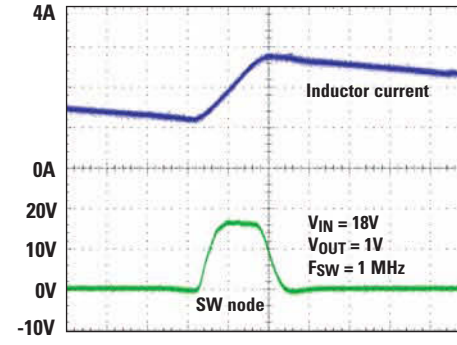

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Design Challenges In Step-Down Regulator Applications

of the diagram shows the normal buck regulator power switching components. The free-wheel diode anode is connected to ground through the controller. A small value current sense resistor and amplifier are used to measure the diode current. The sample-and-hold circuit triggers each cycle, just prior to the turn-on of the buck switch, providing the pedestal portion of the emulated current sense signal.

The LM25576 senses the input voltage and the output voltage to generate a current source that charges an external ramp capacitor (C_{RAMP}). Each cycle when the buck switch is turned on, the capacitor voltage rises linearly. When the buck switch is turned off, the ramp capacitor is discharged. For proper operation, the ramp capacitor is set proportional to the value of the output inductor. A good starting point is to select $C_{RAMP} = L \times 10^{-5}$, where the units of L are Henrys and C_{RAMP} are Farads. The last step necessary to complete the generation of the emulated buck switch current signal is to sum the pedestal information (from the sample and hold) to the ramp capacitor voltage signal. The final result is a controller that behaves like peak current mode control but without the delay and transient effects in the current sensing signal.

For applications operating with duty cycles greater than 50 percent, peak current mode controlled regulators are subject to sub-harmonic oscillation. By adding an additional fixed slope voltage ramp signal (slope compensation) to the current sense signal, this oscillation can be avoided. Referring to the ramp generator circuit, an additional fixed 25 µA offset current provides additional fixed slope to the capacitor voltage ramp signal. For very high duty cycle applications the 25 µA current source can be supplemented with a pull-up resistor or the ramp capacitor value can be decreased to increase the ramp slope, preventing sub-harmonic oscillation.

Overload Protection

The LM25576 output overload protection is accomplished with a dedicated current limit comparator that limits the emulated peak current on a cycle-by-cycle basis. The emulated current mode method provides the added benefit of capturing the inductor current information prior to the buck switch turn-on. If the current pedestal exceeds the current limit comparator threshold, the buck switch skips cycles allowing the inductor current additional time to decay, preventing current run-away.

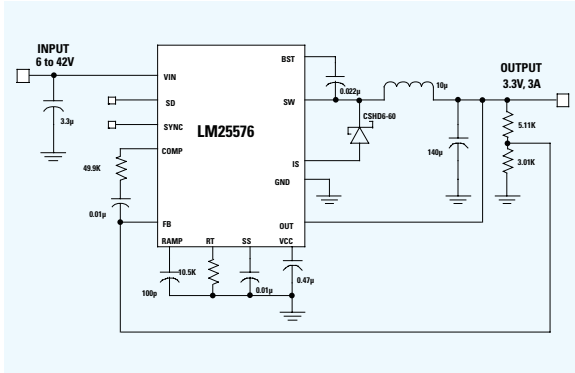

Figure 4. LM25576 Buck Regulator Schematic

Current-mode control offers many benefits. However in buck regulator applications requiring very short on-times the generation of the modulating ramp is very difficult. Through the use of an emulated ramp signal this challenge can be overcome. National has developed a new family of integrated regulators using the emulated current mode control technique.

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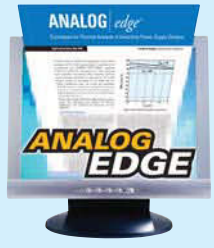

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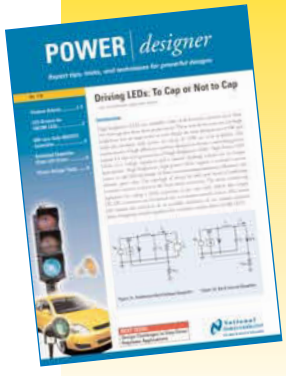

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BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Miller on edge

The last installment of Analog Domain derived the value for the Miller capacitance—the effective impedance between the collector and the base of a bipolar transistor in a common-emitter configuration (**Reference 1**). The derivation shows that the circuit's gain scales the physical collector-base capacitance, C_μ, resulting in the value of the so-called Miller capacitance.

In linear circuits, the Miller term forms a pole by capacitively coupling the stage's output in antiphase to the input. This coupling creates a frequency-dependent negative-feedback term that limits the stage's gain-bandwidth product.

The same physical mechanism affects nonlinear circuits as well. Due to the nature of those circuits' transfer functions, however, the internode capacitive coupling can manifest itself in ways that may not immediately look familiar.

Many high-voltage SMPS (switched-mode-power-supply), motor-drive, and Class-D-amplifier output stages share a common gross topology. This similarity exists despite the diverse parametric requirements these structures must meet.

Though implementations vary, the basic topology is relatively straightforward. A pair of MOSFETs operating as switches alternately connects the output to high- and low-side rails. A timing block generates the control signals that determine the circuit's rms output. The timing controller also ensures that the two switches do not simultaneously conduct by imposing a dead time between the switches' conduction intervals.

The gate-drain capacitance, C_{GD}, is the physical basis for the Miller capacitance in the MOSFET. This parasitic term can affect the behavior of high-voltage switching circuits when the high-side switch turns on to rapidly slew the output node toward the positive rail (**Figure 1**). The positive edge on the low-side FET's drain couples to the gate, and, to the extent that the low-side driver exhibits an ac output impedance, the low-side FET's gate-source voltage, V_{GS}, rises.

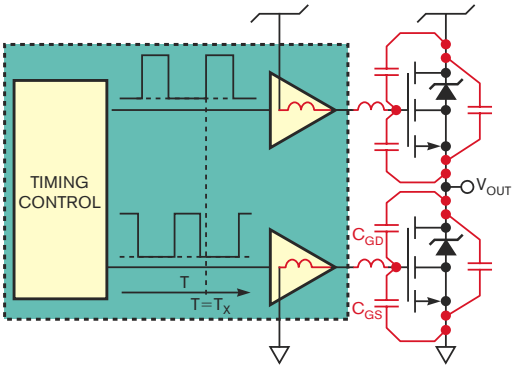

Figure 1 On the rising edge of the output stage, such as at $T=T_X$, the low-side FET can briefly turn on due to a charge that couples through C_{GD}, which degrades the output stage's performance.

If the resultant V_{GS} spike exceeds the device's threshold voltage, V_T, the FET will turn on until its driver can regain control over the gate node. The gate-source capacitance, C_{GS}, mitigates this transient effect, known as CdV/dt turn-on. The transient reduces the operating efficiency of power supplies and motor drives. Audio amplifiers that don't compensate for the output-current error suffer degradation in both harmonic distortion and energy efficiency.

In the limit of driver source impedance and output slew rate, the C_{GS} and C_{GD} terms form a high-frequency voltage divider that attenuates the spike. One of the best ways of preventing CdV/dt turn-on takes advantage of this ac divider.

Power-MOSFET datasheets often carry the typical charge quantities associated with charging the parasitic capacitances to specific voltages. Specifically, Q_{GD} is the charge necessary to raise the C_{GD} parasitic to a specific voltage—often 15V. Q_{GS1} is the charge that the C_{GS} requires to bring the gate to its threshold voltage. To prevent CdV/dt turn-on, a good rule of thumb is to choose a low-side FET with a Q_{GD}-to-Q_{GS1} ratio less than 1.4.

You can minimize the transient turn-on event when it occurs by specifying gate drivers with low output impedances. Also, make sure your product works as well as the paper design by keeping the traces between the driver and the MOSFET gate short. Follow good high-frequency and -current layout practices to minimize stray inductances in the gate-drive loop. EDN

REFERENCE

1 Israelsohn, Joshua, "The Miller's tale," *EDN*, Feb 15, 2007, pg 36, www.edn.com/article/CA6413794.

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BY ROBERT CRAVOTTA • TECHNICAL EDITOR

The smallest change necessary

DANIEL VASCONCELLOS

When I first started working with development of prototypes in field conditions, I inherited responsibility for the legacy test ground equipment. I took care of making any fixes to the system hardware and software as well as adding or changing test and communication capabilities as the flight equipment evolved. As I became more familiar with how the ground and flight systems worked together, I realized I could make the ground-equipment software more flexible and efficient. My technical lead denied my requests to rewrite any or all of the system; his response was always, "Make the smallest change necessary to the system to accomplish what needs to be done."

Being young and inexperienced, I interpreted this response as a lack of understanding of my grasp of the system operation and how I could make it work better. As much as I grumbled about the inefficiency of continuing to use the system as it was, I always ended up making the minimum changes necessary, and the projects moved ahead well enough through all types of technical ups and downs.

We were breaking new technical ground, and we had plenty of opportunities for an in-depth analysis of the failure data when setbacks occurred. We plowed the information we learned from that analysis right into the ground- and flight-equipment software. As the projects advanced, I realized how many lessons learned I was incorporating into the system software.

It wasn't until we handed the project equipment, software, and data to another development team that I realized how valuable those lessons were. At the handoff of the project to the new team, my role changed to that of a third-party-review member. (I learned another lesson in that role that I'll share in a future "Tales from the Cube.")

The new team comprised a set of ambitious engineers who, not unlike my earlier self, wanted to prove how much they could improve on the work of previous teams. This time, though, the team had wide reign to replace and rewrite whole subsystems, which manifested in the team having to relearn some hard-won lessons. When they replaced a subsystem, members failed to take the time to understand why the legacy system did seemingly unnecessary things in apparently trivial conditions. The team not only re-created challenges we had already overcome, but also complicated the failure analysis by changing too many things at once that were codependent on each other.

While living through these avoidable and frustrating episodes, I came to understand the wisdom of my technical lead's responses in denying my requests to rewrite the software just to make it "better." If he had granted my requests, I would have missed retaining some of the lessons that my predecessor learned and incorporated into the software. Further, I probably would have repeated some of the troubleshooting efforts that the previous team had already tackled.

The value of making the smallest change necessary to the system becomes apparent when you are working on a dynamic prototype and pushing the limits of your team's and industry's experience. The time for making the system operate better, without changing function, comes later in the project, when you have a significantly more mature understanding of your system's behavior and have shifted your focus to reducing costs by squeezing out the inefficiencies. EDN

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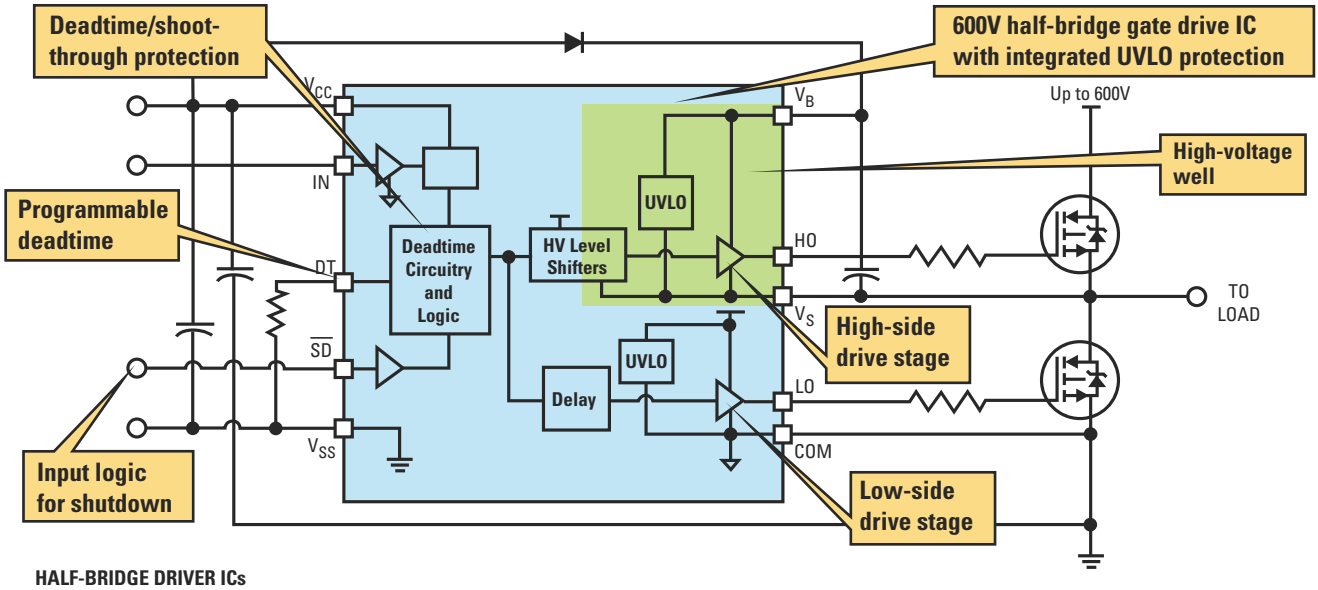

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IRS21084(S)PBF	14	290/600	Programmable deadtime; UVLO V_{CC} & V_{BS}
IRS2109(S)PBF	8	290/600	Input logic for shutdown; UVLO V_{CC} & V_{BS}
IRS21094(S)PBF	14	290/600	Input logic for shutdown; programmable deadtime; UVLO V_{CC} & V_{BS}
IRS2183(S)PBF	8	1900/2300	UVLO V_{CC} & V_{BS}
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IRS2184(S)PBF	8	1900/2300	Programmable deadtime; UVLO V_{CC} & V_{BS}
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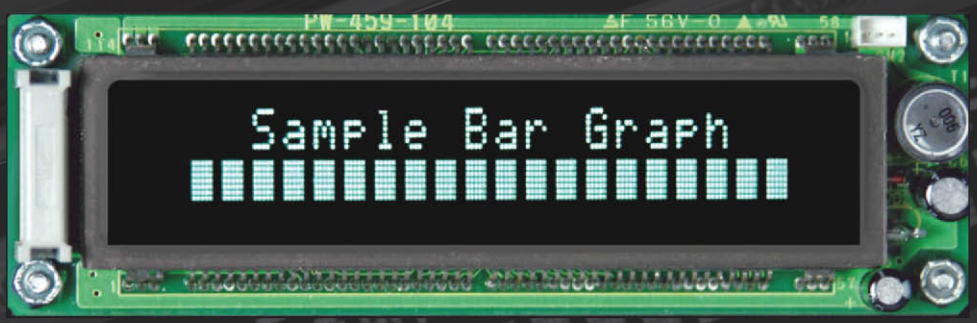

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VARIATIONS IN TEMPERATURE CAN MAKE A CIRCUIT ACT UNPREDICTABLY OR EVEN CAUSE CATASTROPHIC FAILURE. HERE ARE SOME TIPS ON WHAT TO LOOK OUT FOR IN YOUR DESIGNS' REACTIONS TO TEMPERATURE EXTREMES.

Figure 1 This electric-car-motor controller experienced a catastrophic failure (courtesy Otmar Ebenhoech).

HOT, COLD, AND BROKEN: thermal-design techniques

BY PAUL RAKO • TECHNICAL EDITOR

Both heat and cold can have an adverse effect on your circuits. At extremely high temperatures, chips may burn up (**Figure 1**). More commonly, if your design is subject to temperatures you did not expect, many of the parts may fall out of specified limits. When this scenario happens, your circuits may not perform as you would expect. Equally concerning is a scenario in which circuits' temperatures go from hot to cold and then back again. Such situations can cause thermal shock and can even destroy components. Many engineers do not worry about the performance of their circuits at low temperatures, but this lack of concern is a mistake. The performance of semiconductor devices can change dramatically at low temperatures. The base-emitter junction voltage of bipolar transistors rises significantly in low temperatures (**Figure 2** and **Reference 1**). "To design an amplifier that can operate on 1.8V at negative temperatures, you need to consider that V_{BE} [base-emitter voltage] will increase by 130 mV from room temperature to −40°C," says Francisco Santos, product-development-engineering manager at Analog Devices. "This situation will force the designer into a different set of amplifier architectures."

Many amplifiers, such as the Analog

Devices AD8045, speed up when they get cold (**Figure 3**), whereas others, such as the AD8099 slow down when they get cold. "Most of the trouble with cold in bipolar is low-voltage operation," says Bill Gross, now retired, former vice president and general manager of signal-conditioning products at Linear Technology. He says that higher base-emitter voltage and lower current gain make it more difficult to meet specifications. "Lower input impedance and mismatches in beta [current gain] cause bigger problems in the cold," he says, "especially if they are trimmed for room temperature. The higher g_m [transconductance] is easy to compensate for by changing the operating current, but then the slew rate varies."

Low temperatures cause oscillations, instability, overshoot, and poor filter performance. The parts-per-million measurement can change your component values at both high and low temperatures. If you expect the IC die to work from −55 to +85°C, there are only 60° from a 25° ambient to the hottest temperature, but there are 80° from ambient to −55°C. So, make sure that your error budgets examine both the hot and the cold regimes. James McLaughlin, professor of electrical engineering at Kettering University (Flint, MI), says that, as you heat silicon past several hundred degrees, it "goes intrinsic." In other words, the temperatures would get high enough that the dopants would migrate through the lattice, and there would be no more PN junctions, just a block of conducting, impure silicon. Would the bond wires explode, or would the silicon continue to melt until it vaporized?

AT A GLANCE

- Low temperatures can cause more problems than heat.
- Use thermal resistance to calculate chip temperature.
- ESD diodes and temperature probes can help you measure heat.
- Thermal cameras may reveal hidden problems in your design.
- Spice and finite-element-analysis software can help in thermal design.

The damage to ICs running at higher temperatures can be subtler. Martin DeLateur, consultant and former product engineer at National Semiconductor, points out that at temperatures higher than 165°C, the molding compound starts to carbonize. At this point, the molding compound turns into a hard, gray material. Outgassing, the slow release of a gas that some material trapped, froze, absorbed, or adsorbed, causes the release of polymer additives, such as fire retardant. At low levels, this outgassing can impact an IC's short- and long-term operation by adding ions or surface effects to the chip. The bond wires, which may be conducting excessive current, also carbonize the mold compound. This excessive current can cause the hardening of carbon tubes, which might melt the bond wire yet keep it conductive inside the tube. Eventually, the higher thermal expansion cracks the passivation, die, or carbonized-molding compound and causes massive failure. (Military specifications define excessive current as that exceeding $1.2\times105 A/cm^2$; thus, the military insists on hermetically sealed packaging for ICs.) No charring or degradation occurs when there is no plastic on the die. Oil-well-instrumentation companies often test and characterize silicon ICs at 200°C for use in their products. These products have limited lifetime but work far longer than if they were in plastic packages. ICs have shorter lifetimes even when die temperatures are less than 150°C.

In 1884, Dutch chemist Jacobus H van't Hoff first proposed the Arrhenius equation, and Swedish chemist Svante Arrhenius physically justified and interpreted it five years later. In the equation, $k=A_e^{(-Ea/RT)}$, k is the rate coefficient, A is a constant, E_a is the activation energy, R is the universal gas constant, and T is the temperature in degrees Kelvin. Arrhenius initially applied the equation to chemical reactions to describe the speedup of reactions with temperature (**references 2** and **3**). Engineers now also use it to describe the shorter life of electronics when they run at high tem-

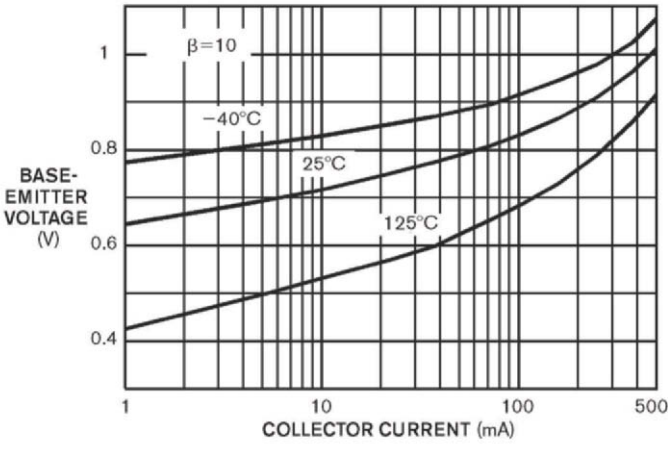

Figure 2 As temperatures increase, the base-emitter voltage of a transistor decreases. At 1 mA, a factor-of-two difference occurs between the voltage at −40 and +125°C (courtesy Fairchild Semiconductor).

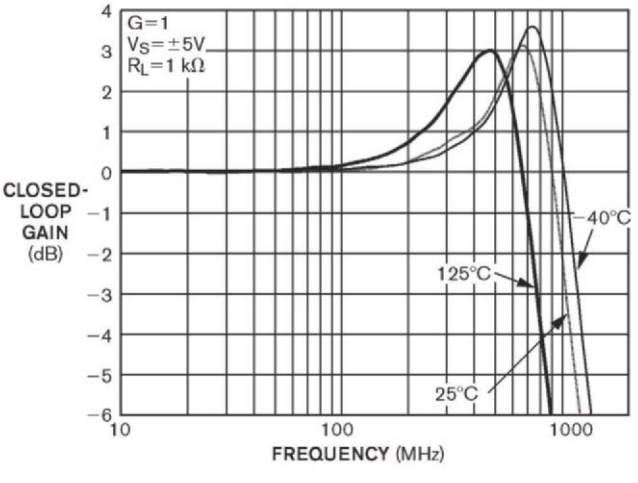

Figure 3 The Bode plot of this amplifier shows that the part is speeding up as it gets cold. There is also an increase in the peaking that would manifest itself as ringing in the time domain (courtesy Analog Devices).

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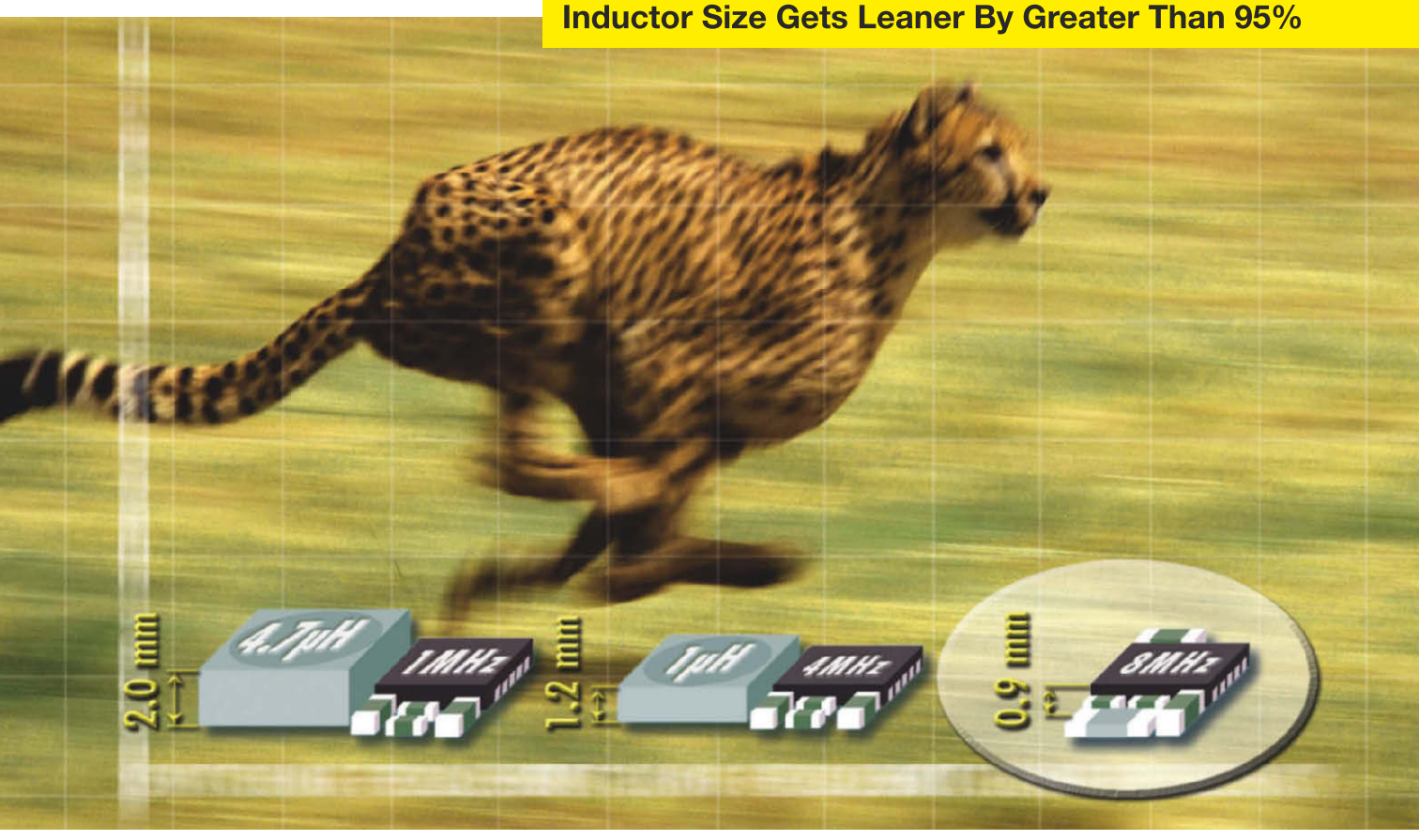

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peratures. The equation implies that every 10°C rise in temperature halves the lifetime of the part. Thus, it is essential to reduce silicon temperatures in your designs. If you can reduce IC temperatures from 85 to 65°C, you quadruple the life of those components.

The cause of problems can be not only the static presence of heat or cold, but also the change from one temperature to another. In extreme cases, thermal shock can rip boards and parts into pieces. Temperature gradients, such as those that create small voltage errors, can also cause problems due to the thermocouple effect of the solder and pin materials (**Reference 4**). Moreover, the temperature gradients themselves can be dynamic. The late Bob Widlar, a pioneering electronics engineer who worked at National Semiconductor, Fairchild, Maxim, and Linear Technology, once received prototype silicon that stopped working at 1 kHz. Widlar discerned that waves of heat were radiating outward from the output transistors. These waves propagated symmetrically through the silicon die. The problem was that the IC had two reference nodes that were unequally spaced from the output transistors. Operating at 1 kHz, one of the referenced nodes was in a thermal trough, while the other was in a thermal crest. This situation so unbalanced the bias circuits that the part stopped working properly. Because of these thermal gradients, some power-supply designers prefer to use controllers rather than ICs with built-in power FETs. With controllers, the heat from the FETs does not wash across the same die and over the amplifiers and reference circuits.

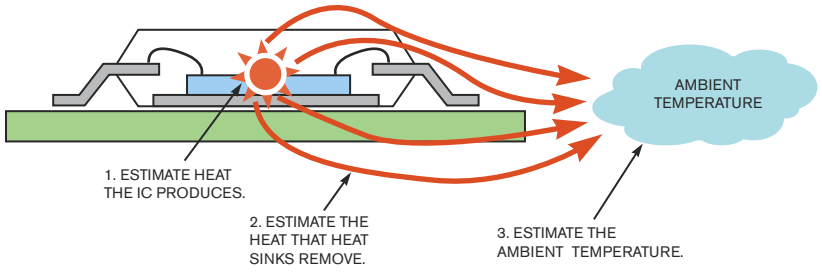

Figure 4 Thermal analysis requires evaluating self-heating inside a part and then estimating the amount of removed heat. Knowledge of the ambient temperature allows the final desired determination: the temperature of the silicon die inside the part as it operates. Heat removal by radiation (not shown) is usually negligible.

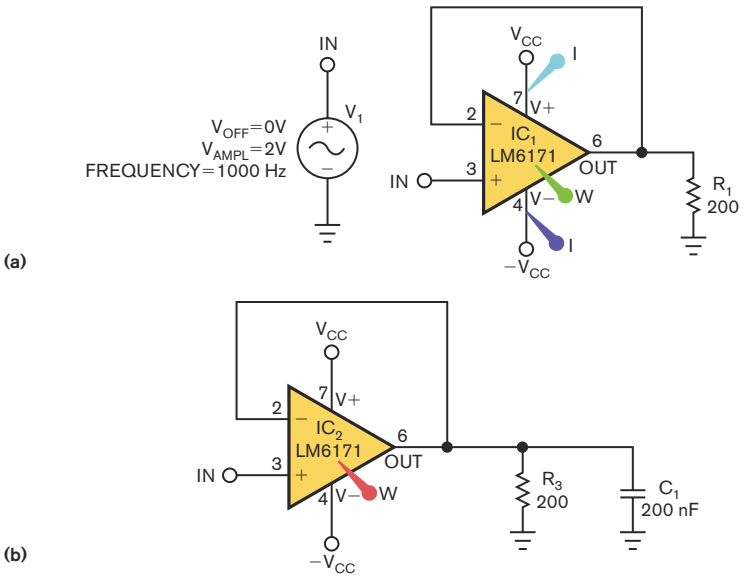

Figure 5 This amplifier circuit—without (a) and with (b) a 200-nF load capacitor—creates the Spice output of Figure 6.

ANALYZING HEAT

Analyzing heat in your circuit is a three-step process. You estimate the heat produced inside the IC. Then, you estimate the heat that the board or heat sink removes. Finally, you estimate the ambient temperature in which the part will be operating (**Figure 4**). DC analysis is often trivial when you are estimating the heat that the component produces: A resistor with 1V across it and 1A going through it produces 1W of heat. Estimating the heat that ac or undefined signals produce is more problematic, however. For one thing, the quiescent current that runs from the power to the ground pin is always dissipating a dc-power term. A part with 10V power rails and 5 mA of quiescent current produces 50 mW of heat. However, under operation, that quiescent current may change somewhat. Bias currents and base-drive currents usually increase when they encounter ac signals. The biggest challenge is figuring out how much heat the output current of the part is creating. This estimation may not be obvious. A part can deliver sizable power to a load, but if the output transistors are either all the way on or all the way off, the power the part dissipates internally will be relatively small. With conventional totem-pole output stages, like those that most amplifiers use, outputting a rail-to-rail square wave is not the most thermally demanding task. The worst-case heat production inside the IC occurs when the part outputs a square wave with an amplitude one-half of the power-supply span. If the part is working on ±12V rails, a ±6V p-p square wave creates the most heat in the output stage. A sine-wave output has lower internal heating. If the signals are complex or indeterminate, it may be difficult to estimate the true worst-case heat production of the IC. Reactive loads with large capacitive or inductive components further complicate the power-dissipation estimation. The voltage and current are not in phase, so the simple assumption about a half-swing square wave becomes false.

You can use Spice to estimate power dissipation if you can characterize the

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PIC24FJ64GA008	80	64	
PIC24FJ64GA010	100	64	
PIC24FJ96GA006	64	96	
PIC24FJ96GA008	80	96	
PIC24FJ96GA010	100	96	
PIC24FJ128GA006	64	128	
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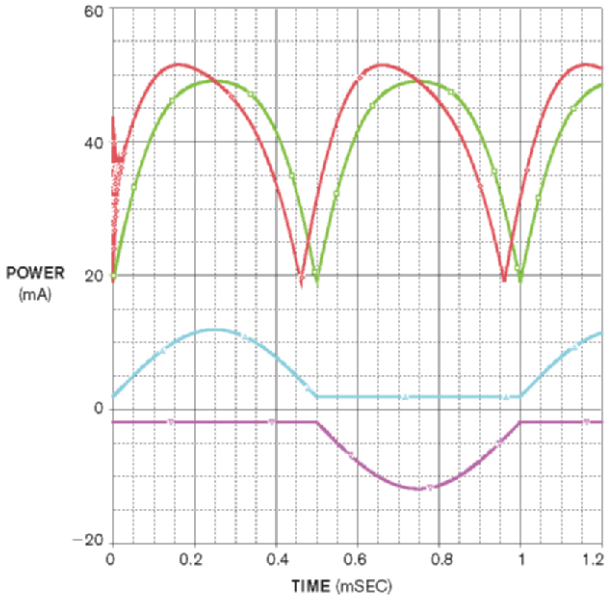

Figure 6 The two lower traces show the currents into the power-supply pins of the upper amplifier. The two top traces show the power that each part is dissipating. The red trace that is associated with the lower amplifier has a higher dissipation due to the added load capacitor. Use the rms function to evaluate the average power.

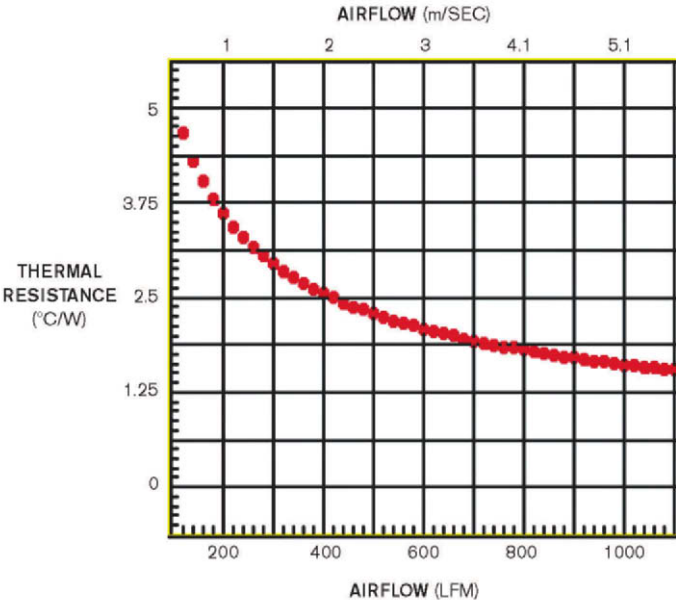

Figure 7 The thermal resistance of a finned aluminum heat sink decreases by a factor of five with forced-air cooling (courtesy Aavid Thermalloy).

signals that the ICs will be passing. You must ensure that the Spice models are proper and that they give reasonable results on a few test signals in which the power-dissipation calculation is trivial. **Figure 5** shows a Spice schematic. The power that the chip dissipates differs from the power that arrives at the load. **Figure 6** is the Spice plot of the schematic in **Figure 5**. It shows oscillation in the red trace at start-up. Whether this oscillation will occur in the circuit is anyone's guess, but it should cause you to look for this behavior after you build the prototype. Bear in mind that clicking the W button in Orcad Capture displays only the quiescent power consumption of the chips. To get the operating power dissipation, use the power markers on the schematic and then use the rms-math function on the plot program to give the average power dissipation in the part.

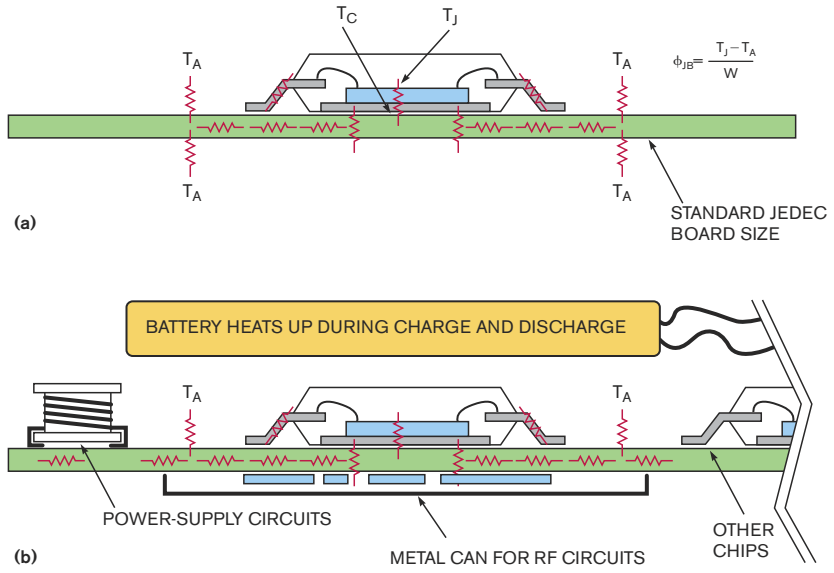

Figure 8 The notation ϕ_{JB} represents the thermal resistance from junction to ambient when a part mounts on a standard JEDEC-defined PCB (a). The addition of a battery, power-supply circuits, a metal can for RF circuits, and other chips causes the IC to run much hotter (b).

The board or heat sink removes heat from your IC through convection, conduction, or radiation. Conduction removes heat primarily through the metal lead frames and board copper. Once board copper or a discrete heat sink spreads the heat, then convection transfers the heat by providing enough surface area for the heat to dissipate into the air. Radiation is rarely a viable method of heat removal. Satellite designers use radiation because no other way exists to remove heat from the system. Because looking out into space presents a radiant temperature close to absolute zero, the temperature differential is large enough to allow a sufficient amount of heat to transfer to space, so the satellite electronics do not burn up.

Convection involves some complications. For example, airflow has an effect on commercial heat sinks (**Figure 7**). Note the five-times improvement in thermal resistance with high airflows. Heat sinks that use forced-air cooling have thinner and more closely spaced fins, as examination of a fan-type CPU

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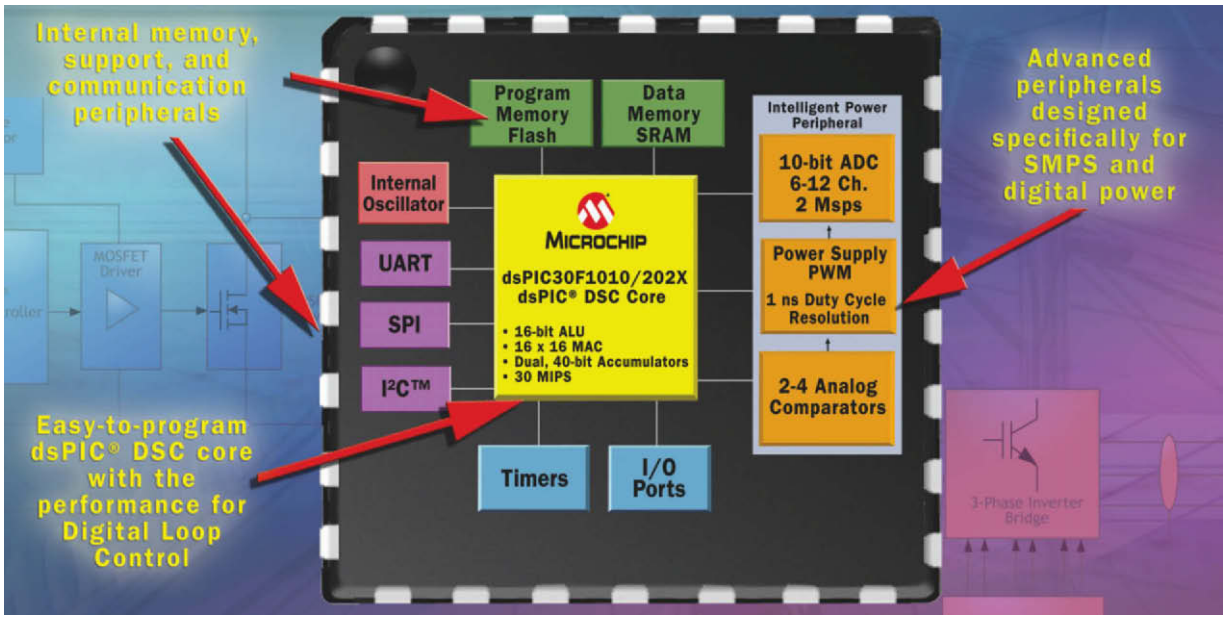

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cooler will prove. If your product has no fan, the heat from your IC will conduct and spread out and then transfer to the air inside the unit. Then, as the whole unit heats up, the heat transfers convectively to the ambient air, along with some conductive transfer if the unit is sitting on your legs. The thermal resistance of the case material then becomes important. A plastic case more slowly transfers heat from the inside to the outside ambient than does a metal case.

Engineers who work on noncabin electronics for fighter jets understand that a jet operates at altitudes as high as 70,000 feet. At that elevation, the air is so thin that convective cooling becomes ineffective. These systems have a cold plate with ethyl-glycol cooling passages that guarantee that the plate will get no hotter than 80°C. Every part physically contacts a metal heat spreader that can take the heat from the components to the edge of the board. At the edge of the board, a thermally effective clamping system presses this heat spreader to the sides of the case. The side of the case takes the heat down to the cold plate on which the case resides. Thermal grease ensures the maximum heat transfer to the cold plate and ensures the maximum transfer from ICs to heat sinks.

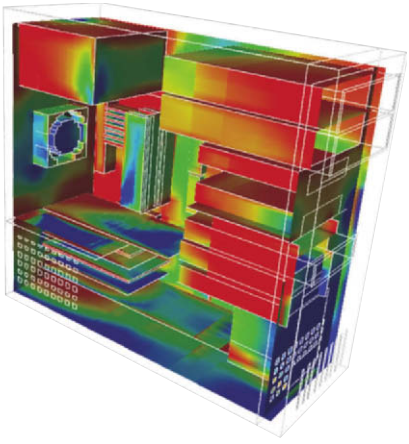

Figure 9 In this thermal simulation of a desktop-computer case, finite-element-analysis software can model both the heat that inside components produce and the heat that airflow removes (courtesy Flomerics).

Most electrical engineers are comfortable with using thermal resistance as a thermal-analysis technique. You express thermal resistances in units of degrees Celsius per watt. You simply multiply the number of watts you estimated in the first step to get the degrees-in-Celsius temperature increase that the part will experience. Several cautions are in order here. Look for the subscripts on the thermal-resistance specification on the part's data sheet. The thermal resistance from die to case, ϕ_{JC}, is not a useful measurement. IC or package designers at the semiconductor manufacturer may care about the IC's temperature rise as heat flows from the die to the case, but you need far more information. The next spec you frequently encounter on the data sheet is the thermal resistance from the junction to ambient, ϕ_{JA}. This value measures the temperature rise when the part is not connected to a heat sink or soldered into a PCB (printed-circuit board). Darvin Edwards, a Texas Instruments fellow, points out that ϕ_{JA} is a useless measurement for most engineers when predicting junction temperature. "What matters is the thermal resistance

from the die to the board [ϕ_{JB}] and the thermal resistance from the die to the package surface [ϕ_{JC}]," he says. "We use two JEDEC [Joint Electron Device Engineering Council]-standard boards to measure ϕ_{JA} to show the engineer it is not a package constant. One is single-sided, and one is multilayer. If you have ϕ_{JB} and ϕ_{JC} specifications, you have a far better chance of estimating a realistic temperate rise of the IC." He also points out that engineers must remember that the ϕ_{JA} measurement takes place with no other chips on the board. When power-supply and other heat-dissipating chips are around the IC and when the board is in a restrictive plastic enclosure with no fan, the actual temperature rise is higher than the ϕ_{JA} measurement suggests (**Figure 8**). Also bear in mind that little heat transfers from the plastic top of most ICs. Epoxy plastic has a 0.6 to 1W/mK (meter-Kelvin) thermal conductivity, and copper has 400W/mK thermal conductivity. Thus, copper is 400 to 600 times more thermally conductive than plastic, and the design of the PCB to maximize thermal conduction is critical.

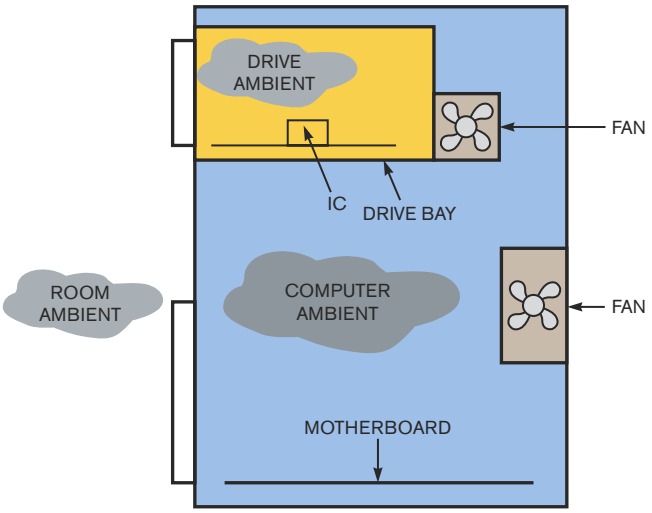

Figure 10 The IC ambient is the temperature inside the CD-ROM drive that surrounds the PCB. That temperature is much higher than room temperature.

More sophisticated methods exist for estimating heat removal from the board. National Semiconductor's Webench online-design tool uses Flomerics' Flotherm thermal-analysis software to calculate part temperatures in still air. All the usual simulation caveats apply. If your circuit has a fan and some airflow, its temperature will increase less. If it has an enclosure and other parts inside, its temperature will increase more. Flomerics uses finite-element-solution

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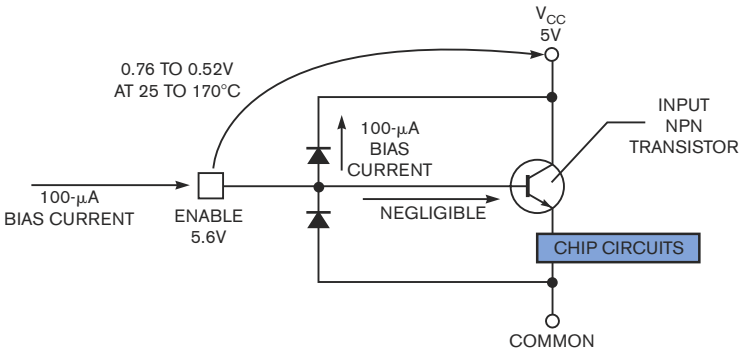


Figure 11 Clever engineers can force a small current into the ESD diode of any IC. The forward voltage is proportional to die temperature even as the part operates. The pin goes above or below the supply rails, but the small, controlled current ensures that the IC suffers no damage.

techniques (**Reference 5**). **Figure 9** shows the result of analyzing a computer case for heat generation and airflow. Many other finite-element solvers can analyze this problem, as well. For example, a solver from Comsol can perform multiphysics, so it can solve partial differential equations for more than one problem, such as the thermal response of a part that has a changing thermal conductivity based on its temperature. TI's Edwards points out that his company provides two levels of thermal-modeling abstraction: ϕ_{JB} resistance and the Delphi-compact-model standard. Flotherm, Icepak, and many other thermal-analysis programs use these models.

The final step in heat analysis, estimating the ambient temperature, is fundamental. A motorcycle with an air-cooled engine undergoes a certain temperate rise over ambient as you drive it. If the ambient air gets 10° higher, so does the cylinder-head temperature. Your electronic system is the same. For example, your chips may operate at 50°C on your lab bench where the air is 25°C. When you place those chips in a 50°C ambient temperature, the chips' temperature will reach 75°C. In this step of analyzing heat, engineers sometimes fail to account for the ambient environment in which their parts may have to work. Aside from simply working, those parts must also survive. For example, the rework-paint oven in an auto plant exposes all the electronics to higher temperatures than they would ever see in a car's remaining lifetime. Mercifully, the parts can survive this treatment because the automaker does not power them up during this process. Many engineers do not appreciate how extreme the environment can get. We all know satellites in outer space can have temperature swings from a few degrees above absolute zero to hundreds of degrees Celsius as they go from the shade to the sun.

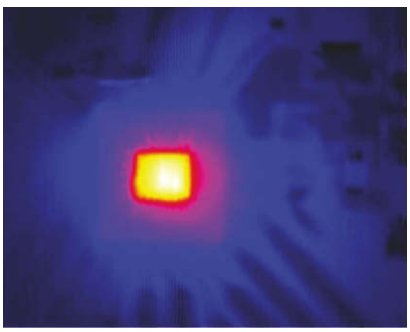


Figure 12 This thermal-camera image of an operating IC die shows a 25°C temperature differential from the edge of the die to the location of the output transistors. The yellow square defines the die, the magenta area shows the bond wires, and the blue area depicts the PCB traces.

Challenging environments abound here on earth, as well. Bruce Robinson, test-development engineer for Nissan America, works at the automaker's desert proving grounds in Arizona. He reports that Nissan generally estimates maximum temperatures as: 46°C ambient day temperature, 81°C interior-air temperature, 111°C maximum instrument-panel-surface temperature, and 82°C interior-component temperature. In other words, you can boil water on the top of the instrument panel. Think about this fact if you design vehicle electronics.

Without question, most engineers trip up when they fail to understand the nested levels of ambient temperature. For example, imagine designing a part

Figure 13 Crusty old lab "rats" call this temperature-forcing system an elephant due to its "trunk" (courtesy Thermonics).

that goes on the optical-pickup unit of a CD player (**Figure 10**). You might assume that, because the part is for a consumer product, it could operate at 0 to 70°C. Think twice. The part on your lab bench may be operating in a 25°C environment. However, the optical-power unit mounts inside the CD drive. Other components inside the drive heat the air. The unit may not have a fan. Even worse, the player resides in a computer. The drive must work in that ambient temperature. The inside of the computer has its own heat sources and fans. The outside-world ambient temperature adds on to all this heat. So, the 25°C ambient temperature you measured on the bench becomes 40°C in the computer and 50°C inside the CD drive. Now, what if you put the computer in a hot upstairs room in Ecuador? The part might have to operate at ambient temperature far above 70°C. It is your job to make sure that it can still meet specifications and that the high temperatures do not radically shorten the product's life.

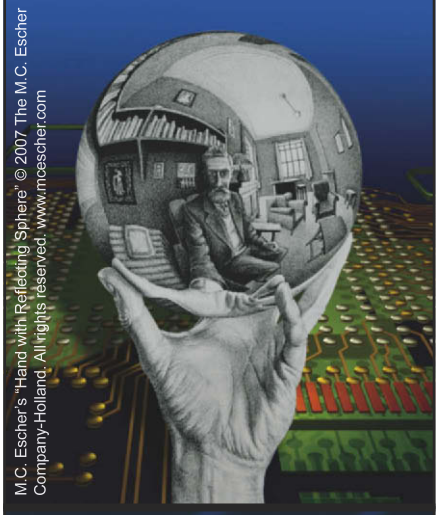
A DOSE OF REALITY

Performing design estimates and Spice simulations is fine, but, at some time in the development process, you must face the reality of what you have designed. Reality involves prototyping the circuit in the correct form, fit, and finish. Then, you can use various measurement techniques to verify all the nice theory you've done so far. It is imperative to recreate the expected operating environment as closely as possible. Your priorities are to determine first whether the circuit will break, then whether it will last, and finally whether it will work as expected in all conditions.

You may recall that a poorly designed and installed in-flight-entertainment system caused the crash of Swissair Flight 111 on Sept 2, 1998 (**Reference 6**). Arcing from wiring of the in-flight-entertainment network ignited flammable covering on insulation blankets and quickly spread across other flammable materials. If the designers at the small company that produced the system had insisted on testing in the 8000-foot-altitude atmosphere of a passenger plane, they would have understood that the disk-drive heads flew closer to the platters and that the heat of the entire system was difficult to remove. TI's Edwards points out that 10,000 feet of altitude reduces the convective cooling of systems by 20%. Verifying that all the engineering assumptions correlate with reality is the only way you can ensure that the design will perform electrically as well as thermally. The 229 passengers on Swissair 111 lost their lives because the in-flight system's designers bypassed this reality check.

Two essential measuring devices for all engineers are their sense of touch and their sense of smell. Most of you are all too familiar with the pungent odor of melted electronics. Those with good olfactory senses can even smell the subtle odor from a chip that is approaching 70°C. You can also put touch to good use on circuits that contain no lethal voltages. If you can hold your finger on the part for more than five seconds, the part's temperature is lower than 70°C. Most people overestimate the heat they sense with their fingers. Often, they estimate a temperature of 70°C when it is only 50°C. If you wet your finger, wipe the part with it, and the part sizzles, you are in trouble, because having any part at a temperature higher than 100°C is bad news. Again, the ambient temperature around your lab bench is the most beneficial environment.

Once you have made rough estimates, you must do some real measurement. Most DVMs (digital voltmeters) have accessories that allow you to connect thermocouples. Fluke and other ven-



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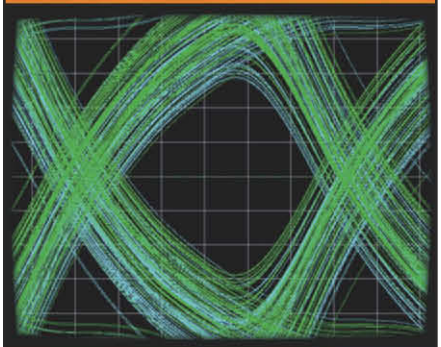

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dors make handheld instruments that accept two thermocouples for measuring the chip along with the ambient temperature around it. You should measure the IC's temperature increase over the ambient temperature. National Instruments, IO Tech, and many other data-acquisition-equipment manufacturers can help you set up measurement systems with hundreds of thermocouples, thermistors, and platinum RTD (resistance-temperature-detector) sensors. Be careful regarding the size of the sensor and the gauge of the wires. When you measure a small IC, the thermocouple wire can conduct heat away, just like a heat sink can, and this conductance lowers the measured temperature. Many manufacturers also offer noncontact-IR (infrared) detectors. When using them, however, note the emissivity of the surface you are measuring. "Emissivity" is a measure of the thermal emittance of a surface—the fraction of energy an object emits relative to that of a "black body," or thermally black surface. A black body is a perfect emitter of heat energy in that it emits all energy it absorbs and has an emissivity value of 1. In contrast, a material with an emissivity value of 0 would be a perfect thermal mirror (**Reference 7**). A shiny metal package has low emissivity and would thus yield a lower-than-actual-temperature reading. Flat-finish black paint has an emissivity of 1, which is the value that IR detectors measure against. To achieve an emissivity value of 1 for your electronics, you can spray them with flat-finish black paint or simply put a piece of clear tape on the metal package, which yields an emissivity value approaching 1.

Many savvy semiconductor manufacturers measure the temperature of the die itself, even when the part is operating in a circuit, using one of the ESD (electrostatic-discharge) diodes that are available on every input, output, and control pin of an IC (**Figure 11**). You can use this method for ICs having reset or CS (chip-select) lines. You can use many other pins for the measurement, as well. Because the forward drop of a diode is directly proportional to current, you can put the chip into an oven and run a small current through the ESD diode. Most people in the industry feel that a current of 100 μA does not cause any self-heating of the diode. You need not power up the part to measure the diode voltage; you can use any input or output pin above the power pin or below the ground pin. The internal ESD diodes on the pin clamp that pin to approximately 0.6V. If the pin is a reset that needs to remain high for the part to work, then pull the pin above the power pin. As the oven temperature increases, the ESD diode's forward voltage falls from about 0.7 to 0.53V. Similarly, if the extra pin is a chip select that must remain low for the IC to operate, you can pull that pin below the ground pin and take your data for that ESD diode. If the pin is an output, check with the manufacturer to ensure no extraneous currents will prevent the full 100 μA from traversing the diode. You must measure this data for each kind of IC you are measuring; different processes have different voltage/over-temperature relationships. When you are ready to measure the IC as it operates in your circuit, you inject 100 μA into the pin to raise it above V_{CC} or pull 100 μA from the pin to drop it below ground. Then, you can measure the voltage difference and infer the die temperature.

The ESD method is valuable but has limitations. If the IC delivers hundreds of milliamperes, voltage drops may occur internally on the V_{CC} or ground-metallization and bond wires. These voltage drops may add to or subtract from your ESD-diode-voltage measurement. You should consult with the application group or even the IC designer if this situation occurs. To counteract the voltage drop, you can stop the power delivery as you are taking the measurement. Be aware that the thermal time constant of silicon chips is microseconds, so you must take the measurement with a fast scope or acquisition system to ensure that you have not measured the ESD diode's forward voltage after the diode has cooled substantially.

Another worry with the ESD-diode method is that IC chips are not isothermal—that is, they do not have equal or constant temperature with respect to either space or time. Measuring the ESD diode does not always ensure that you

have measured the hottest point of the die. The concern here is that the ESD diode, which is always on the edge of the chip, is cooler than the output transistors. You can take an IR-thermal-camera image of the IC die as the IC operates (**Figure 12**). The bright, white spot in the **figure** is a full 25°C higher than the edge of the die where the ESD diode resides. The part may need derating when it operates at elevated temperatures (**Reference 8**). At 150°C, the part may not meet the circuit's needs.

You can use an equally valuable method as the ESD-diode technique to measure the temperature of FETs, even as they operate. This method takes advantage of the fact that the on-resistance of a FET is directly proportional to its temperature. The higher the temperature of the FET, the higher its on-resistance is. By noting the on-resistance at various temperatures, you can infer the temperature of the FET by measuring the voltage across it and the current through it while it operates in the on mode. This method works even for integrated FETs in power-supply chips. Remember that self-heating is always an insidious phenomenon in electronics, so, when you take your on-resistance data in an oven, you must apply a short, fast rise-time pulse current to the FET to ensure that the die is at the same temperature as the oven.

Taking the measurement is just one component of checking reality to verify your assumptions and estimations. You also must create the ambient temperature if it is not readily available. Automobile companies keep test tracks in Arizona and Canada. For electronic testing, a benchtop-test chamber or a temperature-forcing system, such as Thermonics' T-2500E model, may work acceptably (**Figure 13**). Be sure to use cables and test leads that can withstand the heat. Brown BNC cables have higher temperature ratings than the more commonly available black U58 style (**Reference 9**). A quick blast from a heat gun may heat up the IC, but be careful; you can easily destroy a part with a heat gun. Freeze sprays are somewhat safer but have the disadvantage of causing frost to form on your circuit and short-circuit the electronics. Test chambers can create ambient environments, including temperature, pressure, and humidity. You may need all three to fully simulate your ambient environment.

In conclusion, you must keep the hazards of thermal design in mind as you design electronic systems. Be wary of external influences that can wreck your design. Communicate with other engineers who are adding their own circuits that will add heat to or subtract it from your circuits. Just as critically, communicate the thermal issues to the mechanical engineers on the team. They can be your best allies to ensure a good thermal design. And when the manager removes the fan and converts the case from metal to plastic, have your thermocouples and test chambers ready to show him why that is a bad idea. EDN

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WIMAX GAINS IN MOBILE-BROADBAND GAME,

SPRINT NEXTEL, WITH PARTNERS INTEL, SAMSUNG, AND MOTOROLA, WILL DRIVE MOBILE WIMAX FLAVOR IN US BROADBAND DEPLOYMENT.

BY MAURY WRIGHT • EDITOR IN CHIEF

Both notebook-PC users and consumers carrying increasingly powerful smartphones or connected PDAs love wireless-data services. A clear gap exists, however, between relatively short-range wireless-LAN or Wi-Fi (Wireless Fidelity) networks and the wireless WANs that cellular carriers deploy. The cellular networks will never offer the bandwidth of Wi-Fi, and Wi-Fi won't scale to cover entire metropolitan areas. Mobile WiMax (Worldwide Interoperability for Microwave Access) technology, which complies with the IEEE 802.16e specification, can fill the gap—at least from a technology perspective (see **sidebars** "Mobile WiMax and the WiMax Forum" and "Fixed or mobile?"). Less certain is whether WiMax can achieve ubiquity across regions such as North America or even the world. Moreover, everyone from IC vendors to cellular carriers have a different view of WiMax's role both today and as the wireless world moves toward 4G networks.


BUT 4G lurks

Generally speaking, WiMax could achieve anything from spot success to nearly the reach of cellular networks. Presumably, it will offer mobile users a minimum of 1-Mbps services and perhaps 10-Mbps or even greater data rates. Today, WiMax or prestandard WiMax-like networks are serving in developing regions that often lack a wired network. In other instances, WiMax technology competes with cable and DSL (digital-subscriber-line) services. For instance, Clearwire is aggressively building what it terms a WiMax-class network in the United States. Founded by cellular pioneer Craig McCaw, Clearwire is in more than 30 US markets with more than 200,000 subscribers and is in all probability preparing for an IPO (initial public offering). The company matches DSL and cable prices and offers a service with 1.5-Mbps download speeds.

AT A GLANCE

- WiMax will bridge the gap between Wi-Fi and 3G services, providing near the speed of the former and near the reach of the latter.
- Proponents see WiMax as an open-standard wireless service unencumbered by subsidies and service contracts.
- Integrated Wi-Fi and WiMax chip sets for notebooks will ensure that consumers don't have to choose between WiMax and 3G.
- The main obstacle to portable WiMax devices may be the power that the silicon consumes, and the power amplifier may prove especially problematic.

Sprint Nextel, meanwhile, is planning to rapidly roll out WiMax across the United States. The combined Sprint Nextel owns a 2.5-GHz frequency spectrum that the company claims will cover 85% of the households in the top 100 US markets. The company states that it will deploy a network delivering 2- to 4-Mbps rates that potentially could reach 100 million people by the end of 2008. But in the United States, Sprint is uniquely positioned with a widely available spectrum that it can use in a rapid buildup.

WHAT EXACTLY IS 4G?

Sprint's broad plans and Korea's decision to broadly deploy WiMax raise the question of whether WiMax has now become the leading technology candidate for 4G networks—becoming the successor to 3G cellular networks. Indeed, Sprint, Intel, Samsung, and Motorola have used the 4G label in press releases about their partnership and deployment plans. But executives are quick to avoid that term. "I don't want to be the first person who puts a definition on 4G," says Atish Gude, senior vice president of mobile-broadband operations at Sprint Nextel.

Joe Nardone, general manager of Intel WiMax Solutions, agrees, saying, "I hate the description of WiMax as 4G." With the money that Intel has spent backing WiMax, you would think that the company would welcome the 4G moniker and the early lead that WiMax appears to have over other potential 4G technologies. But the 4G label brings with it political, logistical, and technical issues.

Like 2G, 2.5G, and 3G before it, 4G implies an evolution of previous-generation services. A 3G phone will still support older networks, and you might have trouble even finding a 3G connection today in North America. Moreover, the two primary 3G networks have evolved in the CDMA (code-division-multiple-access) and GSM (Global System for Mobile-communications) camps, in each case layered on the 2G frequency bands and the progression of modulation schemes that each side developed. Mobile WiMax is in a significantly different band and uses OFDM (orthogonal-frequency-division-multiplexing) technology.

Some definitions of 4G embrace a dramatic departure from earlier cellular technologies. Peruse Wikipedia's definition of 4G, and you will find objectives such as 100-Mbps data rates and maximum spec-

MOBILE WIMAX AND THE WIMAX FORUM

WiMax (Worldwide Interoperability for Microwave Access) is the name that the industry generally gives to technologies that the IEEE 802.16 standards group defines. The 802.16d standard defines a broadband-wireless scheme for subscribers in fixed locations. The newer 802.16e standard supports mobile-system subscribers. Both standards are broad and full of implementation options. The WiMax Forum is shepherding the technologies to market. The forum has carved out subsets of requirements the standards define to develop profiles such as the WiMax Forum Mobile System Profile. The WiMax Forum also develops conformity tests and certifies conforming products.

Developers of the fixed-WiMax flavor based it on OFDM (orthogonal-frequency-division-multiplexing) technology, which the industry generally recognizes for delivering maximum spectral efficiency (Reference A). Mobile WiMax uses a newer OFDMA (orthogonal-frequency-division-multiple-access) modulation scheme that includes MIMO (multiple-input-multiple-output) technology. The mobile flavor offers greater immunity to multipath interference and includes methods for adapting changing channel conditions–a necessity in a mobile-system market. Mobile WiMax also includes the session management to hand off mobile-system users from one cell to another.

As in many areas, specmanship rules in wireless-WAN technologies. Many believe that Mobile WiMax is capable of 70-Mbps bidirectional data rates. The rate, however, depends on factors such as range and the wireless channel. Moreover, the standard allows service providers to trade off range and capacity or bandwidth. Early on, Mobile WiMax will typically deliver around 10-Mbps rates, and even that speed depends on the number of users in a cell. Sprint Nextel has stated that users on its network will get 2- to 4-Mbps rates.

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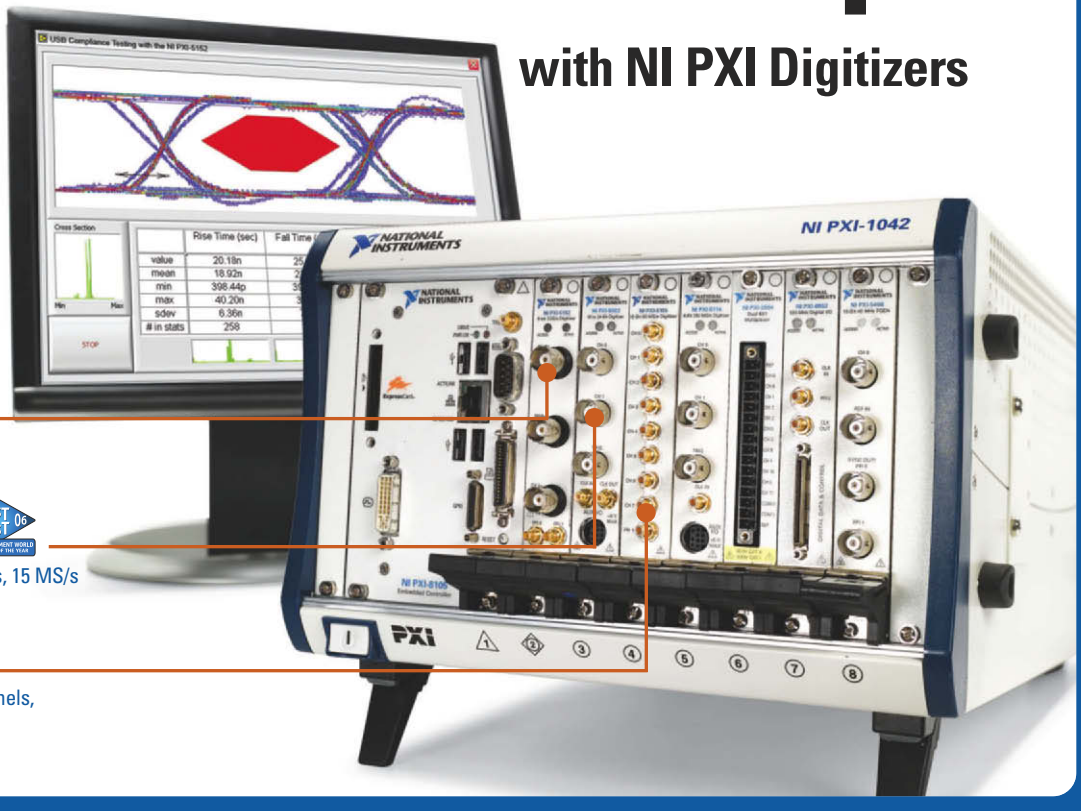

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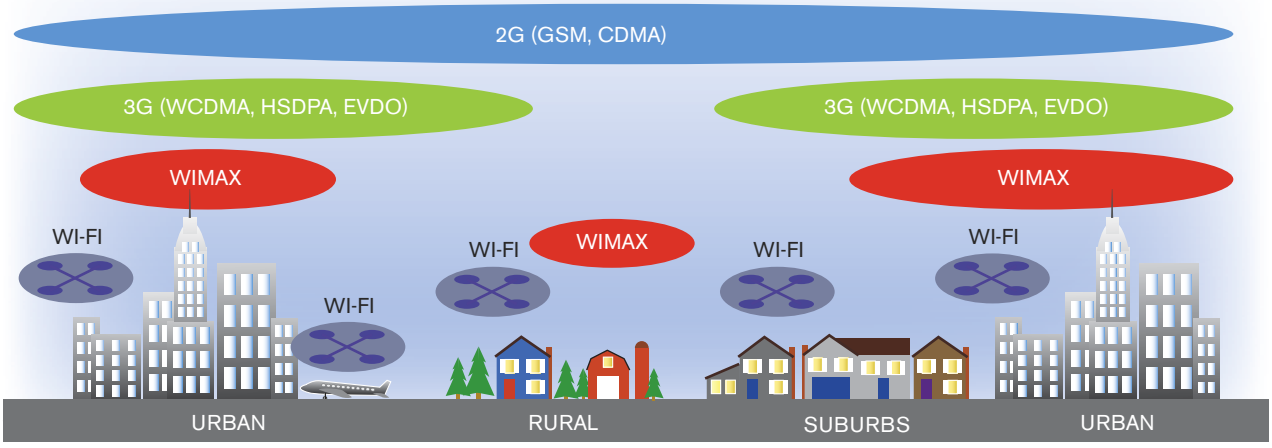

Differing perspectives have Mobile WiMax serving as the 4G successor to today's 3G cellular networks or as a symbiotic technology to cellular systems, with deployment across metropolitan areas but not along roadways between cities.

tral efficiency. Qualcomm has been a dissenting voice, but most experts agree that OFDM is requisite to achieving maximum spectral efficiency, specifically in bits per second per hertz. Moreover, Wikipedia clearly defines 4G as an IP (Internet Protocol) network, with features such as QOS (quality of service) that would support a pure VOIP (voice-over-IP) method for carrying voice traffic.

GOODBYE SUBSIDIES

The business model just may be the biggest issue in labeling WiMax as a 4G technology in the United States. The key WiMax semiconductor suppliers, such as Intel, Wavesat, and Fujitsu in the baseband or SOC (system-on-chip) market, and Analog Devices and SiGe Semiconductor in the radio market, have presented the technology since day one as an open standard. Executives from all of the companies can recite a party line of subscribers buying WiMax devices from their local retailer with no tether to a specific service provider. Even Sprint is emphatic that, with WiMax, it will not go the subsidy-and-service-contract route that prevails in the cellular business.

On WiMax devices, Sprint's Gude states, "We don't want to be the people that control those devices." Gude claims that the subsidy model ultimately adds to the overall cost of a technology.

"Without the subsidy model, the economics of a low-cost data service works," says Intel's Nardone. Moreover, he claims, WiMax users may not even need a service contract. Presumably, users could buy service on an ad hoc or even one-time basis. Gude and Nardone agree that the one-to-one relationship between a device and a service contract won't exist with WiMax.

Without question, Sprint Nextel and its partners Intel, Motorola, Samsung, and, lately, Nokia, are making a bold move with WiMax. It's almost unprecedented for a service provider to announce adoption of such a new technology in one year, roll out initial service in the next, and broadly deploy it in the following. Intel certainly appreciates the high-profile partner given its investment in WiMax. Still, you have to wonder about all of the individual motives coming into play and how the deployment unfolds.

We'll probably never know whether Sprint and Nextel consummated their merger in large part because of some strategic vision on the potential future of WiMax. Or were the WiMax proponents just lucky that Sprint Nextel needed a broadband-wireless technology that perhaps was more attractive from a royalty perspective than other alternatives? More than one prognosticator has opined that WiMax would have died in the United States without the Sprint commitment.

Sprint Nextel had to roll some sort of wireless-data service. As a condition of the merger, Sprint Nextel faced a mandate from the FCC (Federal Communications Commission) to provide

FIXED OR MOBILE?

Ironically, much of the deployment of Mobile WiMax (Worldwide Interoperability for Microwave Access) will serve fixed-system clients. Clearwire focuses on such subscribers, and a desktop modem will be among the first WiMax offerings from Sprint. So, why does the world appear to be coalescing around the mobile flavor? The mobile flavor is more complex than the fixed and therefore presumably more expensive due to a more complex modulation scheme and the requirement to hand off connections from cell to cell. Why won't there be a market for lower cost fixed-system-only implementations?

According to Joe Nardone, general manager of Intel WiMax Solutions, there just won't be enough fixed-only demand to get volumes up and prices down. A single standard will generate economy of scale across the market.

It's also worth noting that, although 802.16e is more complex than 802.16d, the mobile profile that the WiMax Forum specifies is very much a subset of 802.16e. For example, the forum profile specifies only a TDD (time-division-duplex) scheme, in which both base station and client share the same channel for bidirectional communications. The 802.16e spec allows both TDD and FDD (frequency-division duplex), which uses a pair of channels, to carry data in each direction. The mobile profile also specifies relatively few options in frequency bands relative to the broad IEEE specs.

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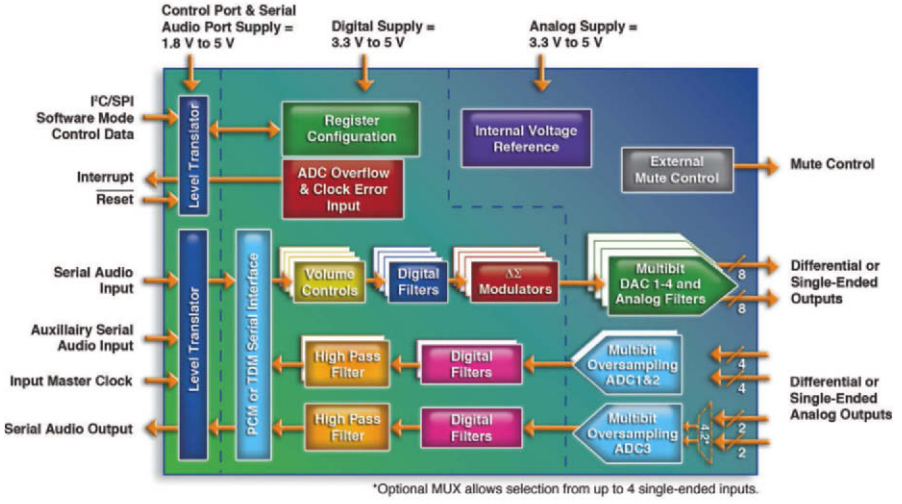

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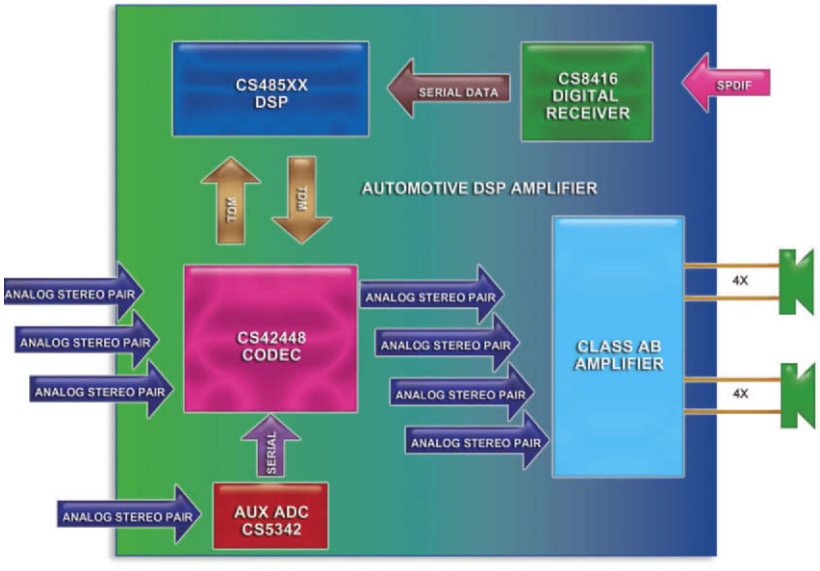

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CS42436/38	105/108 dB DACs; 102/105 dB ADCs	–95/–98 dB DACs; –95/–98 dB ADCs	192 kHz	Single-ended or Differential; 6/8 DACs and 6 ADCs; TDM I/F	52 MQFP
CS42448	105/108 dB DACs; 102/105 dB ADCs	–95/–98 dB DACs; –95/–98 dB ADCs	192 kHz	Single-ended or Differential; 8 DACs and 6 ADCs; TDM and Normal I/F	64 LQFP
CS42888	108 dB DACs; 105 dB ADCs	–98 dB DACs; –98 dB ADCs	192 kHz	Single-ended or Differential; 8 DACs and 4 ADCs; TDM and Normal I/F	64 LQFP

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data services using its broad 2.5-GHz-spectrum licenses by 2009. Nextel was known to have tested OFDM-based technology from Flarion, which Qualcomm acquired in mid-2005.

You won't find executives willing to go on the record to make such a statement, but Sprint Nextel almost assuredly wanted to escape the clutches of the Qualcomm intellectual-property vault. WiMax may have been the only choice Sprint had to meet the FCC mandate or lose those 2.5-GHz licenses. The WiMax move may also give Sprint Nextel leverage in negotiating the use of Qualcomm technology in the 3G market. You can also bet that Qualcomm will claim some intellectual-property rights in the WiMax world. The WiMax Forum has some intellectual-property data on its Web site, but the situation is far from settled concerning who might owe whom once broad deployment starts.

IF MOVING FROM WI-FI TO WIMAX IS AS EASY AS INTEL CLAIMS, YOU WOULD EXPECT THE OTHER WI-FI CHIP MAKERS TO PLAY.

How will Sprint initially deploy WiMax? Sprint's Gude says that the company will start with data cards for notebook PCs and with desktop modems, despite the fact that the technology is, by definition, mobile. The stated goal of reaching 100 million potential users means that Sprint will cover entire metropolitan areas. It will use 3G base-station and antenna locations to collocate WiMax support. But Sprint won't deploy WiMax along, say, freeways between cities, in the way it plans to fully build 3G coverage.

The plan for desktop modems puts Sprint in direct competition with DSL and cable operators. "Sprint could use this [plan] as a push into the home market," says Tom Gratzek, WiMax technical-business director at Analog Devices.

Sprint's Gude disagrees, however. "The target is taking the Internet mobile," he says.

Intel's interest is most assuredly mobile clients—first and foremost, notebook-PC users. "3G is a great start," says Intel's Nardone. "But it's nowhere near making the Internet mobile." On 3G-data services today, he adds, "It's just such a small penetration."

INTEGRATING WI-FI AND WIMAX

So, Intel sees a big gap between Wi-Fi and 3G but, as Nardone further notes, does not want to force users to choose between WiMax and 3G, because WiMax won't have the breadth of 3G coverage. What's the problem with three radios rather than two? Cost is always a factor, but these radios are integrated into notebook PCs using Mini PCI cards, and notebooks typically have two Mini PCI slots. So, Intel is moving to integrate Wi-Fi and WiMax into a single chip set and hopes to ultimately equip every notebook with that chip set.

Indeed, Intel demonstrated a notebook with support for all three networks in December 2006 at the 3G World Congress in Hong Kong. The notebook relied on Intel's new WiMax Connection 2300 chip set, which includes a baseband that supports both Wi-Fi and WiMax and a frequency-agile radio that supports WiMax in the 2.3- to 2.7-, 3.5-, and 3.8-GHz bands. That radio should support the bands in which vendors may deploy Mobile WiMax worldwide.

Both Wi-Fi and WiMax use OFDM, making the integration possible. Moreover, the two technologies operate in similar spectrums and can even share the same antenna. Intel has not priced the new chip set. The company claims that the design is complete and plans to ship it late this year. Frankly, Intel just needs to be ready for when Sprint rolls out WiMax next year.

Ironically, the other Wi-Fi leaders, such as Atheros, Broadcom, and Marvell, haven't discussed WiMax plans. But, if moving from Wi-Fi to WiMax is as easy as Intel claims, you would expect the other Wi-Fi chip makers to play. The other key WiMax-baseband-chip vendors include Fujitsu, Sequans, Picochip, and Wavesat.

Does it sound as if WiMax now can't miss in the United States? Not so fast. There are issues ranging from affordable and low-power silicon, to whether Sprint can deliver on the network deployment, to the competition (see **sidebar** "Portables demand power-miserly chips" at the Web version of this article at www.edn.com/070329cs).

Qualcomm is quick to present an argument that evolving technology in both the GSM camp, which 3GPP (Third-Generation Partnership Project) leads, and the CDMA camp, which 3GPP2 (Third-Generation Partnership Project 2) leads, will serve mobile-broadband needs better than WiMax. Peter Carson, senior director of product management at Qualcomm CDMA Technologies, points out that 3GPP HSPA+ (high-speed-packet-access-plus) technology will soon offer downlink rates as fast as 28 Mbps. HSPA+ is an enhancement to and a combination of HSDPA (high-speed-downlink-packet access) and HSUPA (high-speed-uplink-packet access). Carson even claims that CDMA EVDO (evolution-data-optimized) Revision A will offer better data rates per channel than Mobile WiMax.

Carson claims that the evolved cellular networks will outperform WiMax, especially when you judge them on the minimum data rate they guarantee at a cell edge. He further claims that the cellular system has more efficient connection-management techniques. Finally, he points out that Mobile WiMax uses a TDD (time-division-duplex) scheme to send traffic in each direction on one channel, and cellular-data offerings all use FDD (frequency-division duplex) and a pair of channels for simultaneous upstream and downstream transmission.

No one in the WiMax camp buys Qualcomm's argument. In fact, the WiMax Forum has an in-depth comparative analysis on its Web site that presumably shows the spectral advantage of OFDM over CDMA. Even Sprint Nextel, which plans to support both technologies, claims that WiMax delivers at least a fourfold improvement in spectral efficiency, along with lower cost than CDMA technology. Of course, the cellular carriers are all doing well selling data cards for notebook PCs. Those 3G network extensions aren't yet carrying much voice traffic, but they soon will. The WiMax proponents inevitably point out that more voice capacity was still the reason behind the move to 3G technology.

The 3GPP and 3GPP2 groups are also working on longer term OFDM-based schemes—presumably for 4G—while improving 3G networks. The 3GPP group has developed LTE (long-term evolution), and the 3GPP2 has developed UMB (ultramobile broadband), both similar in concept to Mobile WiMax. The developments are too early to gauge the potential of success.

MORE AT EDN.COM

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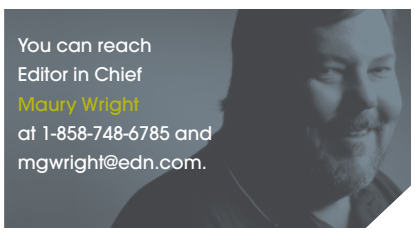
Meanwhile, the cellular and WiMax players are set to collide. The close Sprint WiMax partners—Intel, Samsung, Motorola, and Nokia—insist that WiMax is simply a better fit than cellular technology in serving a host of new persistently connected consumer products. The group cites products such as portable game consoles and digital cameras as likely targets for WiMax connections. Qualcomm has been especially vocal about similar products and has even announced the Snapdragon chip platform to target just such technologies. Meanwhile, Motorola, Samsung, and Nokia are poised to add Mobile WiMax support into handsets, and Samsung is already selling such products in Korea.

Korea was supposed to be the early WiMax proving ground. Korean companies and the government were quick to adopt a technology that would free them from the Qualcomm royalty burden. But the early Mobile WiMax, or WiBro (wireless-broadband), news in Korea has been mediocre at best. In the past, Korea has been a consistent early adopter. Gratzek from Analog Devices speculates that the prevalence of 3G services and fiber to the home in Korea probably hurt the WiMax uptake.

Japan is next up in demonstrating the possibility of WiMax's future success. The government is preparing for a spectrum auction for wireless broadband. Intel's Nardone claims that four of the five participants are committed to WiMax technology. Still, Japan could have the same problem as Korea, given Japan's fiber-to-the-home program and enthusiastic 3G-user base. EDN



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Efficient simulation and validation for mixed-signal SOCs

ADDING ANALOG CONTENT TO DIGITAL-IC DESIGNS CAN BE A NIGHTMARE. SIMULATION AND VALIDATION TOOLS CAN HELP WARD OFF THE TERROR.

The IC-design groups tackling complex digital-IC projects often have problems attaining complete system coverage of their designs. But when they add analog content into their designs, attaining coverage becomes a nightmare because no comprehensive method exists for directly validating an entire design. The ever-rising popularity of cell phones and assorted wireless interconnects has reinvigorated the use of RF and analog circuits. Consequently, mixed-signal SOCs (systems on chips) are here to stay. Unfortunately, that means the complexity of top-level validation is also here to stay.

Designers now attribute the most common errors in SOCs to a mix of human error and a lack of comprehensive validation. The most commonplace errors in this vein are errors in interconnection, failure to test all possible modes of operation, polarity inversion of control signals, and errors with transposed digital buses. You can also attribute a lot of these problems to a lack of a single comprehensive validation method.

IC design has traditionally been in two camps: analog and digital. Designers build most digital circuits behaviorally in RTL code with automated synthesis and most analog circuits using TLD (transistor-level-design) tools—including schematics and a Spice tool. Neither method is completely ideal for full system validation. Design validation in Spice is painstakingly slow or simply doesn't converge, whereas digital simulators have no graceful way of dealing with analog- and mixed-signal functions.

You can approach the simulation and validation problem in a number of ways, all having strengths and weaknesses. However, design complexity and the amount of analog versus digital components make some methods impractical.

ALL ANALOG

In an all-analog approach, you use a Spice simulation, which defines everything as transistors. The all-analog approach works well for small designs, sub-blocks of a larger system, or individuals with lots of time to waste. Low-dropout regulators, op amps, comparators, and other commodity ICs come to mind here. Professional versions of Spice, including Cadence's Spectre, Mentor Graphics' Eldo, Synopsys' HSpice, and Simucad's SmartSpice (www.cadence.com, www.mentor.com, www.synopsys.com, www.simucad.com), all attempt to speed things up. However, most SOC designs require a lot of simulation. Design and transistor-model complexity are outpacing computer speeds for simulation. Consider that the BSIM (Berkeley Short-Channel IGFET Model) 4.2 transistor model has more than 230 parameters, and designs with 1 million transistors are part of the challenge. Spice's ability to simultaneously solve equations and do floating-point math prevents quick simulations of these complex structures. When you add corner testing and multimode operations into the mix, the all-analog methodology is simply not viable.

However, the analog methodology is still viable for developing the small analog sub-blocks in an SOC. Also, any necessary frequency-domain analysis must remain all-analog due to the fact that designers simulate digital systems only in the time domain.

ALL-ANALOG, FAST SPICE

To help speed analog development, a number of companies have developed "fast-Spice" tools. These tools expedite

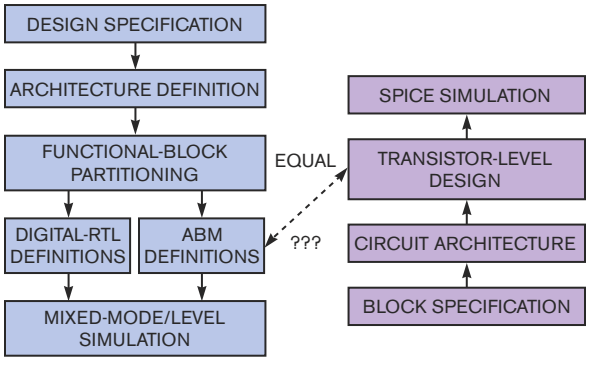

Figure 1 Designers today typically employ a top-down (left) or a bottom-up (right) design method.

simulation but sacrifice accuracy. Common fast-Spice techniques include: model simplification, relaxing error tolerances, lookup-table methods, event-driven methods that ignore inactive circuits, hierarchy, better simultaneous equation-solving methods, variable time-steps, and design partitioning. Most tools interactively trade accuracy for execution time. Designers can make adjustments depending on the accuracy they require for a given portion of the design they are simulating.

However, at the heart of the method, the tools define all the circuits at the transistor level. This approach might improve simulation time, but any significant digital content or large amounts of analog circuitry make this method quickly nonviable. Anything with digital gates should use RTL-simulation methods. Thus, fast-Spice tools are more valuable as part of mixed-mode-simulation methods.

MIXED MODE

In mixed-mode simulation, designers define analog circuits as transistors and digital circuits as RTL. This method is viable in limited situations but often chokes if your design contains a significant amount of analog content. Virtually any transistor-level content greatly slows the process. Early analog/digital co-simulation products comprised two simulators with a method of transferring information between them. Some simulators attempt to improve speed and ease of use, but, no matter how you configured them, number crunching with Spice makes things run slowly. Designs employing a mix of ADCs, DACs, and PLLs do not simulate efficiently with this method, but this approach is valuable when you are developing smaller, mixed-signal blocks. Designing an ADC with digital and analog parts is a good example.

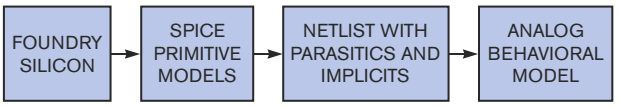

Figure 2 Designers need to ensure that silicon correlates to Spice models, Spice models correlate to a simulation netlist, and Spice simulation correlates to an ABM.

With no efficient way to simulate larger designs with transistor-level tools, the design industry developed ABMs (analog behavioral models), such as Verilog-A, Verilog-AMS, and VHDL-AMS, to speed simulation. Generally, for a large SOC, this approach is the only one in which execution time is viable. Minimizing the need for floating-point math, removing the use of complex-transistor models, and providing functional definitions that sidestep the details of transistor-level implementation all combine to expedite simulations. Accuracy of the behavioral model is a manageable concern. In this method, each ABM needs to have a validation path back to the TLD. System-level designers perform most first-pass ABMs to a mathematical ideal.

Indeed, behavioral modeling and simulation have become new disciplines within the design community with conferences and working groups addressing the needs and issues associated with these disciplines (**references 1** and **2**). Design entry is currently language-driven, with Verilog-A, Verilog-AMS, and VHDL-AMS being the dominant tools. The use of HDL-based tools implies that the orientation is to the digital designer who writes code. Successful analog simulation requires knowledge of the subtle aspects of circuits, and many analog designers don't want to write code. The solution for this problem is simple although not readily available: a schematic-entry tool for ABM development. Conceptually, this tool would be similar to The MathWorks' (www.mathworks.com) Simulink environment, which serves as a tool for the creation of Matlab code (**Reference 3**). One start-up (**Reference 4**) is attempting to develop such a tool, so options are becoming available. Designers, depending on their preference, will most likely use either the HDL or the schematic methods. For now, however, designers wishing to use ABMs need coding skills. The skills are easy to acquire, and numerous examples are available to help designers get started (**Reference 5**).

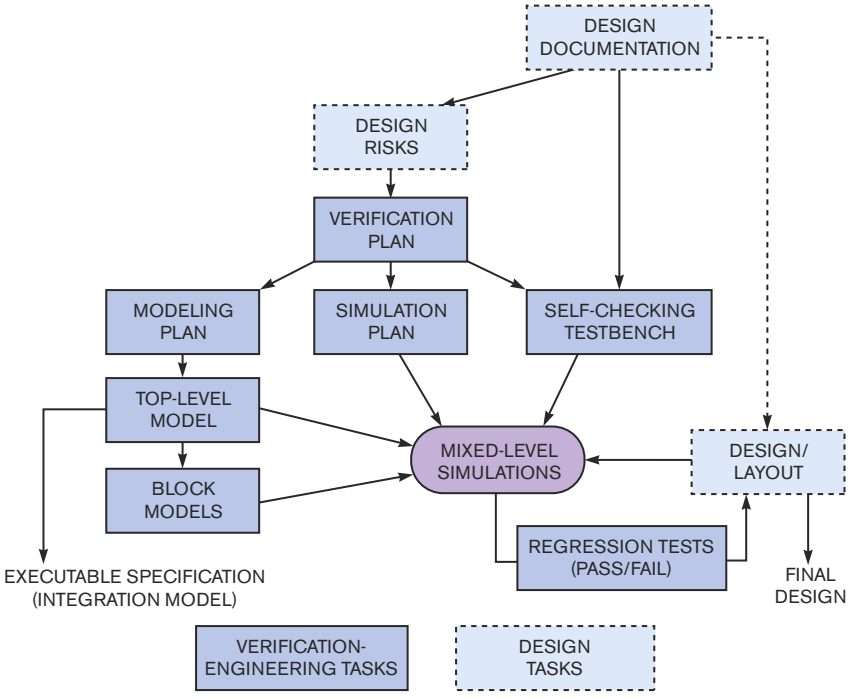

Figure 3 Designer's Guide Consulting's Ken Kundert has an approach that includes use of automation and a complete set of ABMs, which results in a more efficient process.

MIXED LEVEL AND MODE

Using a mix of ABMs, TLD, and RTL digital becomes both mixed-mode and

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mixed-level simulation. This type of simulation is a useful approach because it allows you to behaviorally expedite things while optimizing TLD. The behavioral blocks help create the testbench for the transistor-level section. For example, when designing a charge pump in a PLL, using an ABM voltage-controlled oscillator and an RTL-feedback divider considerably expedites simulation. Being able to close the feedback loop allows easier optimization of the device.

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The selective use of ABMs during this process implies that a full set of these models will be available as the block-by-block design nears completion. With these models in place, designers can do a fully behavioral top-level simulation. With complex designs, designers should avoid using transistor-level design at the top level.

CURRENT-MODE SIMULATION

A technique for determining timing delay in digital designs, current-based modeling, does not apply to analog design, because simulation tools need to solve all fundamentals, including Ohm's Law, Kirchoff's Voltage Law, Kirchoff's Current Law, V=LdI/dt, I=CdV/dt, I=dq/dt, and q=CV, for full Spice accuracy. According to CK Kumar, product-marketing manager at Nascentric (www.nascentric.com), current-based modeling is "valuable for analog behavior of digital circuits" but does not provide a complete analog-design-tool set, as most Spice tools do.

TOP DOWN VERSUS BOTTOM UP

Designers today typically employ a top-down- or a bottom-up-design method (**Figure 1**). The two approaches usually come from different types of designers. Top-down design gets a lot of buzz about being the "correct" way to develop chips. In this method, designers develop a block-level architecture with RTL or ESL (electronic-system-level) functional definitions and first-order ABMs for analog- and mixed-signal structures. The typical top-down designer works from either a system or a digital perspective. Designers have been successful using the method for large SOCs, but the weakness in top-down design is that designers must validate the ABM-to-analog-TLD correlation and frequently are unaware of the nonideal nature of the TLD.

Bottom-up design suits TLD, in which designers manually piece together each functional block to create amplifiers, ADCs, and PLLs. This method far predates the SOC era, when transistor counts and area were small enough that designers could simulate them in a reasonable time with Spice. All mixed-signal chips combine top-down and bottom-up methods. Even if designers use a top-down approach and purchase their mixed-signal IP (intellectual property) from a third-party vendor, someone did TLD for those boxes. So both approaches are valuable and needed. The important thing is getting them to properly meet in the middle with an accurate ABM to represent the TLD.

ABM-TO-TLD CORRELATION

Designers need to ensure that silicon correlates to Spice models, Spice models correlate to a simulation netlist, and Spice simulation correlates to an ABM (**Figure 2**). All of these items are issues because lack of correlation breaks the chain necessary for maintaining accuracy. Many problems arise from inaccurate foundry models, and designers frequently omit implicit items from simulation netlists, such as package and bonding models, component mismatch, noise parameters, and parasitic coupling, and the Spice model, consequently, is either incomplete or inaccurate.

The step that is most often troublesome, especially when digital designers are using a top-down approach and analog designers are using a bottom-up approach, is Spice simulation to ABM correlation. Designers often overlook a mismatch in this step. An all-too-common example of this omission occurs when an "ideal" DAC in a top-level design runs well through simulation. But when the design undergoes manufacturing, the DAC causes large current spikes on the power when it is clocking, or it takes too long to power up.

Much debate exists in the industry about the amount of design detail and quality designers need to make sufficiently accurate ABMs. For example, an ABM modeling a synchronous interface to the digital core—an ADC or a DAC, for example—may require only a simple model that validates the interconnect, the response to digital controls, and ideal operation. Designers can initially use Spice analysis to gain data on the detailed performance of the block. Designers then must use the ABM to validate control polarity and proper interconnect within the SOC. Designers can derive ABM definitions directly from the bottom-up-design process of multimode and multilevel simulation. Running a testbench with TLD and ABM while developing subsections of a design can give designers an interactive comparison of the two models. Top-down design implies that design teams have created an ABM before TLD takes place, so designers must ensure that the final ABM and TLD plug and play in the same way.

Designers can add even more characteristics to ABMs to quantify the interaction of blocks and ensure that their ABMs thoroughly validate their designs. Some industry participants think that design teams should even create transistor-level ABMs, but others see transistor-level ABMs as redundant. Going to this level of detail puts designers in the "too-complex-to-simulate" cage from which they are trying to escape. They need an accurate, functional black-box model. Beyond digital interconnect and ideal functioning, designers can add other components to their black-box ABMs to improve their quality. For example, they can add loading and source impedances—both entering and leaving the box—to ensure that the model provides a reactive impedance similar to the TLD. Latency is another factor, because a delay always occurs from the input to the output of a circuit. A delay similar to that of the TLD is appropriate. Undetermined state periods, including mode switching, PLL-acquisition times, and the like can lead to "output-not-stable" scenarios. A complex model could mimic these conditions, but conditional error flagging during those periods should suffice. Designers need to check power cycling in the TLD for suitable behavior. After that, the ABM can use error flagging for a predetermined period whenever the power supply

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or a power-down control changes state. Designers need to create conditional statements that monitor the acceptable range of power and ground voltages. These languages support the concepts of "analog events" and "event monitoring." In addition, conditional statements monitor the stimulus and loading of the pins of the ABM block. The intent is to provide enough information to validate interconnection and proper functions. Designers need to check each small block in Spice, as well, and to balance the model's complexity with how much simulation time they need to run the more complex models.

SYSTEMATIC TESTING AND VERIFICATION

If designers use top-level verification, they must keep track of multiple models of the same blocks, model correlation, multiple modes of operation, multiple testing scenarios, revision control, and the associated database management. Depending on the complexity of the design, designers may find that manually performing these tasks can be error-prone, cumbersome, or simply impossible to track. Consulting with an expert on how to either streamline or fully automate the process seems a wise course of action. Ken Kundert, one of the founders of Designer's Guide Consulting (www.designersguide.com), specializes in the verification of large mixed-signal chips. While at Cadence, Kundert led the development of Spectre, SpectreHDL, and SpectreRF. He has also been involved in the definition of Verilog-AMS, Verilog-A, and VHDL-AMS modeling languages. Due to the complexity of the process, Kundert's approach includes use of automation

DESIGNERS NEED TO CHECK EACH SMALL BLOCK IN SPICE AND TO BALANCE THE MODEL'S COMPLEXITY WITH HOW MUCH SIMULATION TIME THEY NEED TO RUN THE MORE COMPLEX MODELS.

and a complete set of ABMs, which results in a more efficient process (**Figure 3**). Kundert's approach maximizes the use of software automation, because validation coexists with, rather than is merely a part of, the design flow.

Key concepts in the methodology include a verification plan that defines the models, modes of operation, input stimulus and acceptable outputs; a modeling plan that defines the necessary HDL and ABM models; and a top-level model that becomes an executable specification, which demonstrates the functions and features of the final chip. The methodology also includes a simulation plan that itemizes the tests to be run, the appropriate configuration in each test run; a self-checking testbench for model selection, providing stimulus and response monitoring and parametric pass/fail decisions; and regression testing to ensure that design progress and modifications do not corrupt design integrity and to swap small TLDs with ABMs so that model correlation remains unbroken.

You can find a comprehensive description of these concepts

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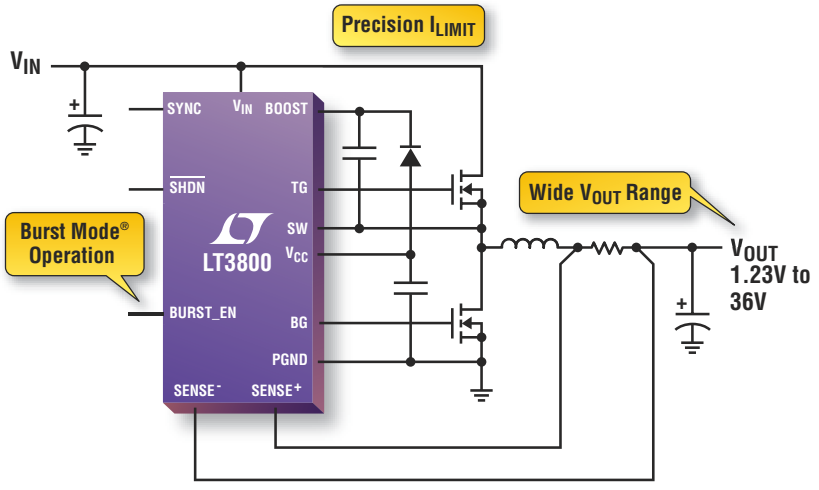

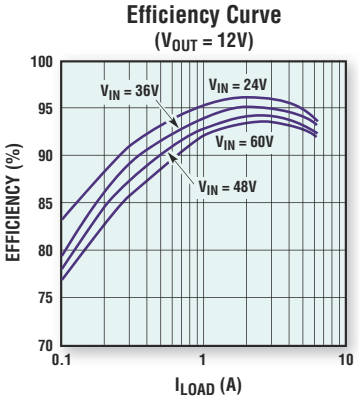

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LT3724				80	-	200	Fixed 200kHz Operation
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LT3845				120	100 to 600	100 to 500	
Switchmode Monolithics							
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LT3434	2.5	3.3 to 60	1.25 to 0.9 x V_{IN}	100	230 to 700		

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on the Designer's Guide Web site, but note that it provides only top-level validation. If you use the approach, you need to run TLDs through a complete set of tests before bringing them into the top-level system. The approach does not consider process, voltage, temperature, statistical variance, mismatch, noise, and linearity. Using the approach requires designers to broaden their skills, write models, and understand control and test and verification definition. Designers who lack these skills can hire validation specialists; doing so is more cost-effective than multiple design re-spins.

INSUFFICIENT SYSTEM VALIDATION AND TOP-LEVEL CHIP VALIDATION NOW CAUSE MOST PROBLEMS IN SOCs.

In conclusion, insufficient system validation and top-level chip validation now cause most problems in SOCs. Spice-level validation is more accurate than using simplified ABMs, but Spice simulation is too slow, and most design groups lack the computational power necessary to make it practical to boost Spice simulation and make transistor-level validation of large SOCs. Instead, designers are now developing methods to validate their large designs. A popular choice is to use ABMs, which range in complexity from simple, ideal structures to highly detailed Spice equivalents. Of these ABM approaches, perhaps the most effective is the black-box equivalent in which the ABM and TLD have similar stimulus-response characteristics.

Designers can effectively perform ABM-to-TLD validation on much smaller blocks. For SOCs, however, they should bring the system together with ABMs and multimode, multilevel methods. Doing so ensures viable simulation times and the ability to run multiple simulations at the top of the design. Automating the validation as a separate procedure outside the design flow is a valuable way to expedite the process, reduce errors, and provide a greater probability of success. EDN

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Jerry Twomey is the founder of Effective Electrons (San Diego CA), where he is responsible for IC-product development, including consulting, training, seminars, design services, and technical support. Twomey received bachelor's and master's degrees from the Worcester Polytechnic Institute (Worcester, MA). His personal interests include sailing, photography, hiking, camping, and inline skating. You can reach him at jerry@effectiveelectrons.com.

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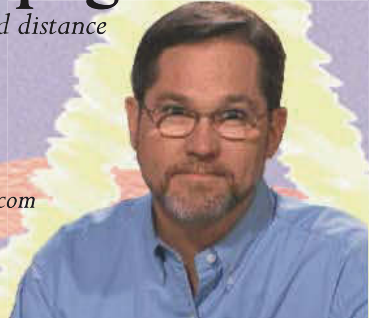

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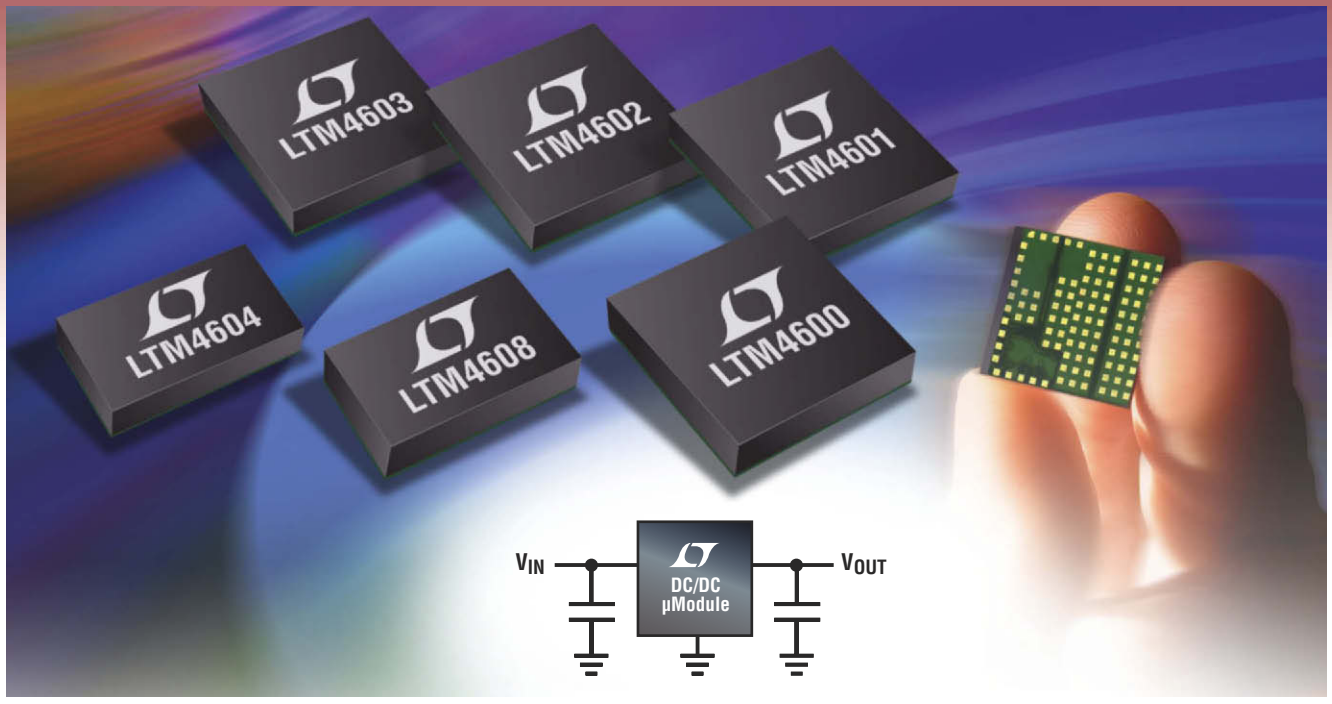

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LTM4600	10A						
LTM4601	12A		✔	✔	✔		
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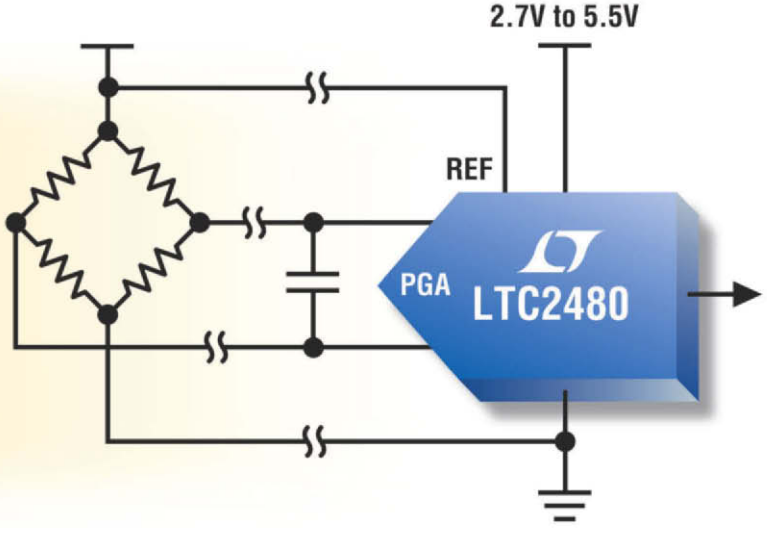

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LTC2483	16-Bits	I²C	1		7.5Hz	3mm x 3mm DFN-10	$1.65
LTC2484	24-Bits	SPI	1	Yes	7.5Hz/15Hz	3mm x 3mm DFN-10	$2.45
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designideas

READERS SOLVE DESIGN PROBLEMS

Oscilloscope helps obtain Bode plots in non-50Ω environments

Antonio Eguizabal, Freescale Semiconductor Inc, Tempe, AZ

A Bode plot can simplify characterization of an active or a passive network by showing frequency and phase representations of the network's transfer function, T. In its classic form, a Bode plot graphs frequency data on an X-axis logarithmic scale and amplitude and phase data in logarithmic or linear format on the Y-axis scale. However, most network analyzers' input ports typically present fixed, low impedances of either 50 or 75Ω that load any device under test that connects to the ports. To measure passive or active circuits in environments other than 50 or 75Ω, you can buffer the analyzer's inputs with amplifiers that present high input impedances to the device under test and low output impedances that match the network analyzer's inputs.

As an alternative to building or purchasing custom buffer amplifiers, you can use the near-ideal amplifiers in an analog oscilloscope that provides a vertical amplifier output on its rear panels—for example, the venerable Tektronix (www.tektronix.com) 465B. Its more commonly available cousin, the Tektronix 2465, provides a Channel 2 output on its rear panel. This Design Idea describes a proven measurement method that obtains magnitude and phase graphs of both active and passive devices. A Bode plot displays the magnitude $|T(j\omega)|$ as a function of angular frequency, $\omega=2\pi f$.

Most measurements span a broad range of frequencies, and it is thus helpful to present the frequency data in logarithmic format (log f) on the graph's abscissa (X axis) and amplitude data formatted as $20\log(|T(j\omega)|)$ on the ordinate (Y axis). Two graphs of magnitude and phase versus frequency thus present a compact representation of the network's electrical characteristics. Using the analyzer's controls, select the magnitude of S21 and phase of S21 as Y-axis displays in rectangular coordinates and select the log f display option for the X axis.

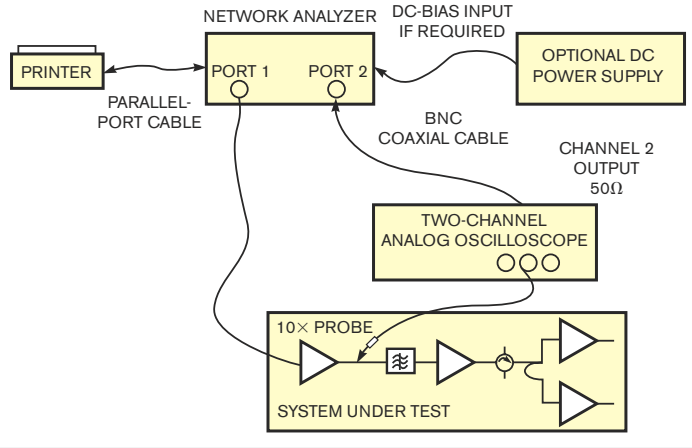

Figure 1 The basic test setup for generating Bode plots requires a network analyzer, an analog oscilloscope with one or more vertical outputs, an optional dc-bias power supply, and a printer.

A Tektronix 465B or 2465 oscilloscope's vertical amplifier presents a 100-MHz bandwidth, a 1-MΩ input impedance, and a 50Ω output impedance. Connect the scope's low-impedance output to the network analyzer's Port 2 input. A 10× probe that connects to the oscilloscope can raise its effective input impedance to as high as 10 MΩ. Oscilloscopes other than those mentioned or stand-alone amplifiers can deliver wider bandwidths, higher dynamic-input-voltage range, and reduced phase error and group delay for more accurate measurements. **Figure 1** illustrates the basic measurement configuration. Use coaxial cables with appropriate connectors to match the network analyzer's inputs. If the network analyzer requires dc bias for Port 1, use an external power supply.

For best results, calibrate the system as follows.

1. Perform the network analyzer's

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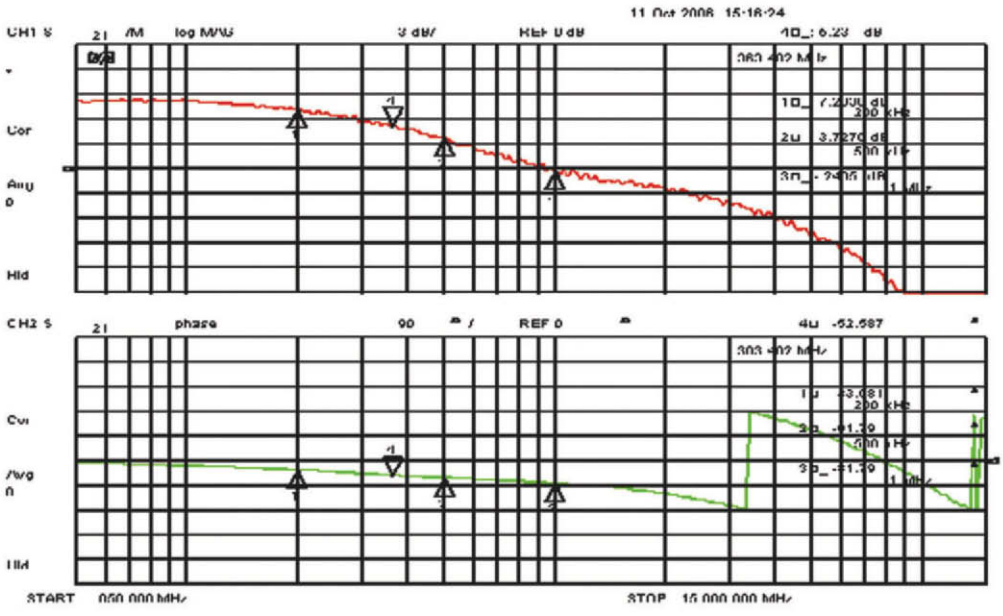

Figure 2 A vertical amplifier with 100-MHz bandwidth fairly accurately measures a device under test operating at 10 MHz, plotting the magnitude (top-trace) behavior and phase (bottom-trace) behavior of a typical device in log-frequency format spanning a 50-kHz to 15-MHz range. Markers show measured values at reference points.

two-port calibration procedure over the frequency range of interest.

2. Set the network analyzer to produce a dual display, with the magnitude of S21 on top and phase of S21 at the bottom of the display screen. Change the frequency-display mode from linear to log.

3. Set the oscilloscope for dc coupling and center its trace at midscreen. Select the required sweep rate and the triggering mode to ac and adjust the trigger level to produce a trace.

4. Connect the oscilloscope's Channel 2 input or probe to the network analyzer's Port 1 input and set the analyzer's controls to establish a reference line.

5. Adjust the vertical amplifier's gain and attenuation (volts/division) controls until the analyzer displays random noise, which represents the lowest detectable signal.

6. Set the analyzer's gain-per-division scale to 3 dB/division, a convenient value for determining the frequencies at which the gain of the device under test decreases by 3 dB.

7. Adjust the network analyzer's source (output) power range in decibels referred to milliwatts and the oscilloscope's gain/attenuation settings in volts per division to obtain an optimum data display. If the device under test introduces appreciable gain or loss, adjust the analyzer's scale-reference control to recenter the displayed trace. **Figure 2** shows a Bode plot derived from an active device that would not tolerate analyzer loads of less than 10-kΩ impedances.

To minimize the phase shift that the oscilloscope's vertical amplifier introduces, choose an amplifier whose bandwidth greatly exceeds the operational bandwidth. In **Figure 2**, a vertical amplifier with 100-MHz bandwidth fairly accurately measures a device under test operating at 10 MHz. You can eliminate phase-shift and amplitude errors that the test fixture introduces by storing a reference trace and subtracting it from the active trace. Refer to the network analyzer's operating manual for details. EDN

PRBS generator runs at 1.5 Gbps

Lukasz Sliwczynski, AGH University of Science and Technology, Institute of Electronics, Krakow, Poland

PRBS (pseudorandom-binary-sequence), or PN (pseudonoise), generators find a broad range of applications in digital-data transmission (**Reference 1**). These circuits often comprise simple shift registers with feedback that can serve as test sources for serial-data links. As their name implies, the output sequence is not truly random and in fact repeats after 2^N-1 bits, where N denotes the shift register's length. Polynomial notation, in which the polynomial order corresponds to the shift register's length and, thus, the PRBS' period provides a convenient method of describing the sequence.

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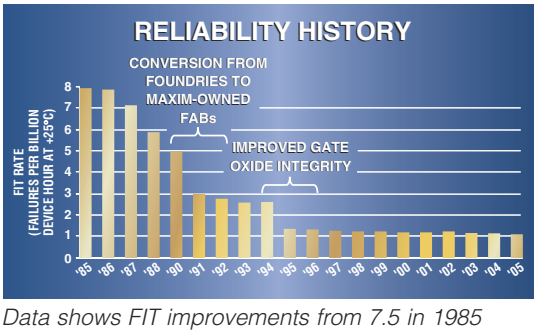

Data shows FIT improvements from 7.5 in 1985 to 1.1 in 2005.

Photo courtesy NASA/JPL-Caltech.
*The Cassini spacecraft uses Maxim's high-speed ADC.

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Communications-equipment tests use certain standard polynomials. For example, x^7+x^6+1 yields a PRBS period of 127 bits, $x^{23}+x^{18}+1$ yields a period of more than 8 million bits, and $x^{31}+x^{28}+1$ yields a period that's 256 times longer. A PRBS with a longer period generally produces a greater variety of data patterns that more thoroughly check the transmission system's performance.

A simple shift register with feedback from an intermediate stage can generate a PRBS. The flip-flops constituting the register must run at a speed equal to the transmission speed, which may pose a problem if you want to build a long-period PRBS generator that runs at a gigahertz clock rate. A high-speed serializer such as Texas Instruments' (www.ti.com) TLK2201B, which runs at data rates as high as 1.6 Gbps, offers one potential solution to the problem. However, instead of accepting a PRBS in its natural fully serial format, the serializer accepts only 10-bit portions at a time.

The circuit in **Figure 1** illustrates a 31st-order, parallel-PRBS generator that delivers 10-bit output segments and can easily adapt to other PRBS orders and output widths. To design the circuit, begin by drawing a diagram with 31 flip-flops arranged in rows containing nominally 10 flip-flops. In this instance, the design comprises four rows, with only one flip-flop in Row 1. **Figure 1** shows the timing relationships among the flip-flops and the numbering convention.

The resulting structure forms a parallel shift register, with the fourth row fed directly from the third row, the third fed from the second, and so on. Flip-flops 10 through 2 in Row 2 and flip-flop 1 in Row 1 receive their inputs from the feedback path. This arrangement ensures that flip-flops in consecutive rows always deliver their outputs 10 time instants apart, and the generator's clock thus runs at one-tenth the speed of an equivalent serial-shift-register PRBS implementation.

To determine the feedback signals, derive the equation that describes a standard—that is, serial—

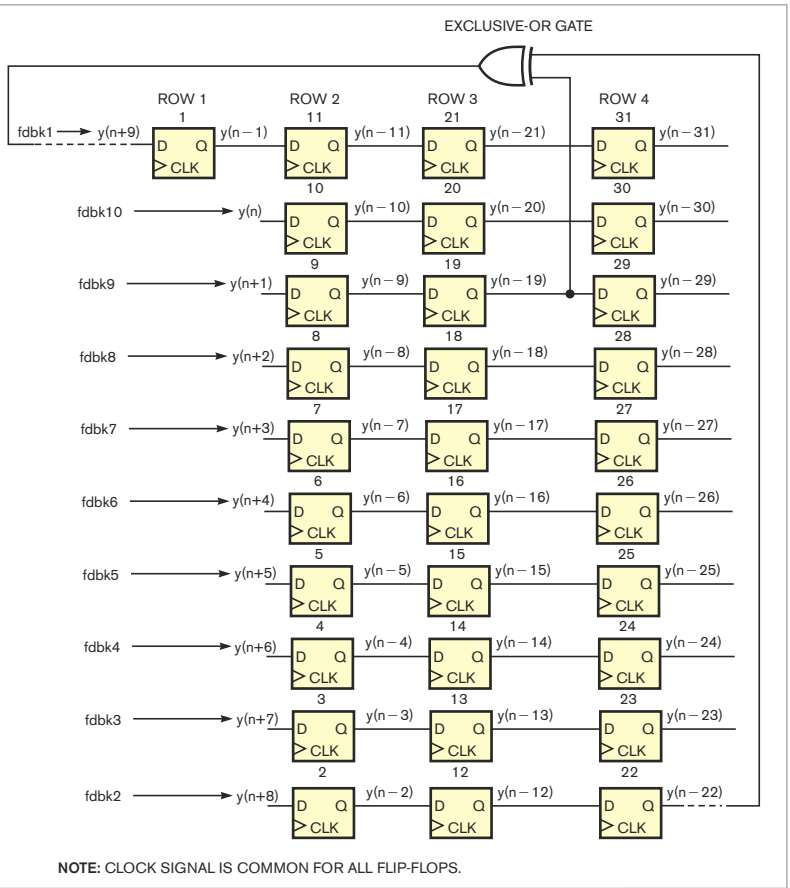

Figure 1 This circuit implements a 10-bit parallel-output PRBS generator defined by the polynomial equation $x^{31}+x^{28}+1$. To reduce clutter, the schematic shows only one of 10 exclusive-OR gates that generates the register's feedback signals. A common clock source (not shown) drives all 31 flip-flops' clock inputs.

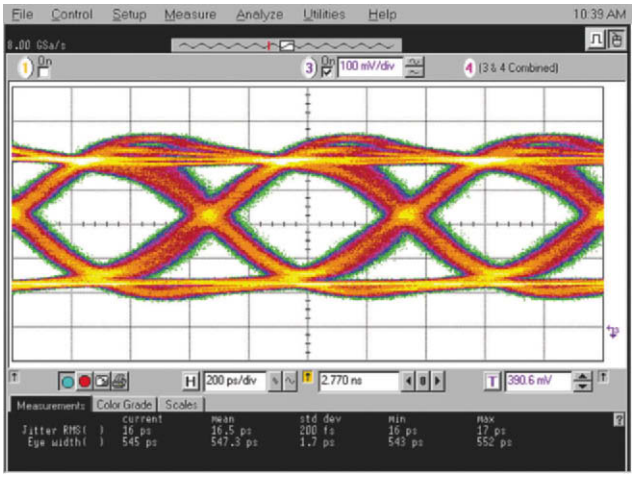

Figure 2 A pseudorandom sequence produces this eye diagram as measured at the output of a TLK2201B serializer that an FPGA-sequence generator drives.

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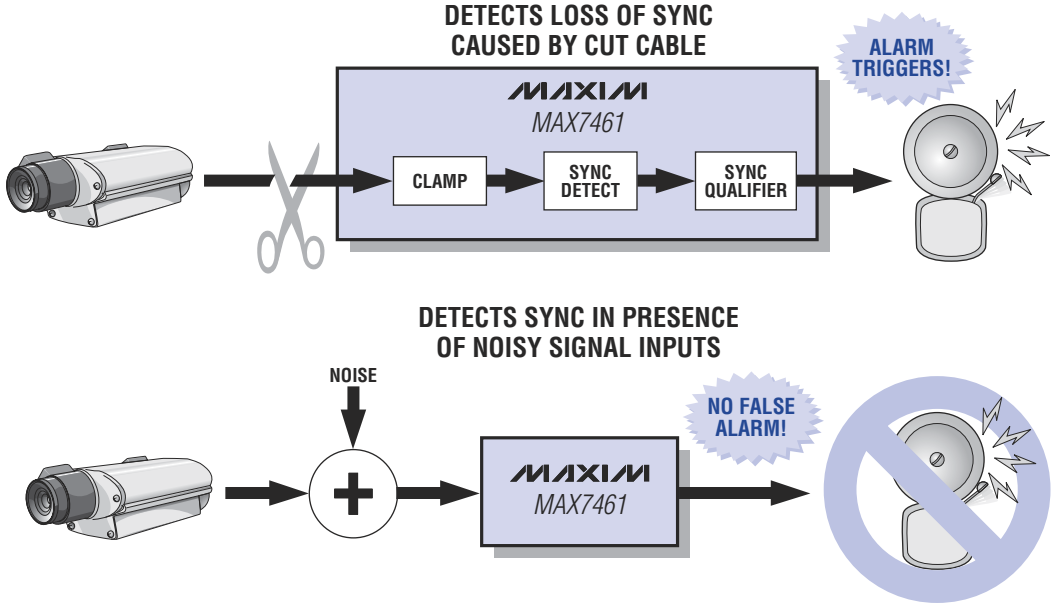

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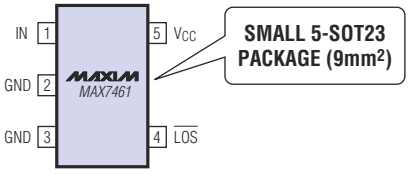

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PRBS generator's output, which, for a polynomial of $x^{31}+x^{28}+1$, yields: y(n)=y(n−31) xor y(n−28). Using that equation, you can derive the equations that describe feedback signals fdbk1 through fdbk10. That is, fdbk1: y(n+9)=y(n−22) xor y(n−19), fdbk2: y(n+8)=y(n−23) xor y(n−20), … fdbk10: y(n)=y(n−31) xor y(n−28). For example, feedback signal fdbk1 derives from the output of a two-input exclusive-OR gate driven by the outputs of flip-flops 22 and 19.

Listing 1, which is available at the Web version of this Design Idea at www.edn.com/070329di1, contains the VHDL code that implements the circuit of **Figure 1** in either a CPLD or an FPGA device. Lines 15 through 18 define the parallel-shift register, and lines 21 through 23 define the feedback circuit's construction. The circuit in this Design Idea fits into an XC3S50 Spartan 3 device from Xilinx (www.xilinx.com), runs at a 150-MHz clock rate, and drives a Texas Instruments TLK2201B serializer at 150 MHz through a 10-bit interface. Xilinx's ISE 7.1i software compiled the circuit's VHDL files. **Figure 2** displays an eye diagram for the serializer's output and confirms the circuit's operation at 1.5 Gbps. The compilation software predicts that the circuit should run at clock rates exceeding 300 MHz, but the TLK2201B limits operation to 150 MHz. EDN

REFERENCE

1 Miller, Andy, and Mike Gulotta, "PN generators using the SRL macro," Application Note APP211, Xilinx Inc, June 15, 2004, www.xilinx.com/bvdocs/appnotes/xapp211.pdf.

Use SystemVerilog for coverage metrics

Thomas L Anderson, Cadence Design Automation, San Jose, CA

The design-and-verification industry is at the intersection of two important trends in the design and verification of SOC (system-on-chip) devices: the adoption of SystemVerilog HDVL (hardware-description and -verification language) and the increasingly critical role for coverage metrics. The interest in SystemVerilog is understandable; this IEEE-standard language has the features for RTL (register-transfer-level) design, high-level modeling, testbench creation, and assertion specification (**Reference 1**).

SystemVerilog also provides constructs for design-and-verification engineers to specify functional coverage points—conditions that designers must exercise for complete verification of the design. Designers increasingly use functional coverage to supplement traditional code coverage. The primary driver for this evolution is the widespread use of constrained-random-stimulus generation.

Traditional verification plans typically include a list of design features or tests that verify features and test status. This approach has worked well with handwritten, directed tests because of the clear correspondence between features and tests. However, verification consists of writing and running each test in simulation, perhaps after turning on some code coverage to help identify features you may have missed in the plan.

Constrained-random-stimulus generation requires a different approach, in which each automatically generated test can exercise many features and parts of the design. A modern verification plan lists features, functional coverage points for the features, and coverage status. You gauge verification closure by the number of coverage points you exercise rather than the number of tests you complete.

SystemVerilog provides all the features necessary to develop both handwritten tests and constrained-random testbenches and to track progress toward closure. Most simulators have built-in code coverage for the new design constructs that SystemVerilog introduces. Thus, code-coverage metrics are available for designs taking advantage of the language's advanced RTL features.

SystemVerilog provides several powerful specification methods for functional coverage. The first is cover property, which is part of the SVA (SystemVerilog Assertions) subset of the language. SVA's assertion features, including temporal sequences, are also available for functional coverage. For example, **Listing 1** ensures that the simulator exercises the two extremes—one and five cycles—of a request-acknowledge handshake. Both simulators and many formal-

LISTING 1 MINIMUM AND MAXIMUM RESPONSE

```
minimum_response: cover property (@(posedge clk)
          (req ##1 ack ));
maximum_response: cover property (@(posedge clk)
          (req ##5 ack ));
```

LISTING 2 PAYLOAD SIZES OF INCOMING PACKETS

```
covergroup payloads_seen (@(packet_received);
     coverpoint payload_size {
          bins empty = { 0 };
          bins minimum = { 1 };
          bins maximum= { 1023 };
          bins others = default; }
endgroup : payloads_seen
```

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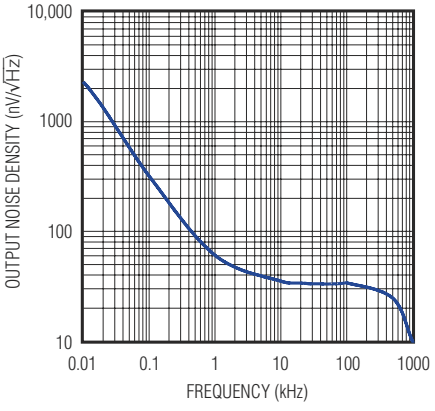

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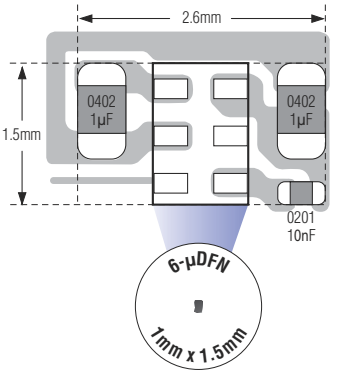

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analysis tools support the cover-property construct. If formal analysis can prove that a coverage point is unreachable, a design bug may be blocking important functions from being exercised. If formal analysis instead provides a trace showing how to reach a coverage point, this trace can provide a good hint on how to write or generate a test.

LISTING 3 ENUMERATED TYPE FOR FOUR PACKET CLASSES

```
enum { read, write, atomic, ctrl } packet_class
covergroup packets_seen (@(packet_received);
     coverpoint payload_size {
          bins empty = { 0 };
          bins minimum = { 1 };
          bins maximum= { 1023 };
          bins others = default; }
     coverpoint packet_class;
     cross payload_size, packet_class;
endgroup : packets_seen
```

Beyond individual coverage properties, you sometimes must track ranges of values. SystemVerilog provides the cover-group construct, which is not part of SVA, to perform this function. For example, **Listing 2** tracks the payload sizes of incoming packets on a network interface and ensures the coverage of corner cases of empty, minimum, and maximum payloads. SystemVerilog also provides the cross construct to measure cross-coverage between two coverage points. This feature allows the tracking of combinations of coverage metrics. For example, **Listing 3** specifies an enumerated type for four packet classes for the network interface, adds a cover point to track the packet classes, and crosses the packet types with the payload sizes.

Ultimately, the SOC-tapeout decision must take into account all coverage metrics. Although functional coverage is the primary method, code coverage has value as a backup to identify areas of the design with no functional coverage due to an incomplete verification plan. The project team needs to merge together code- and functional-coverage results to assess verification progress and help determine verification closure. Coverage is critical for modern, constrained-random verification. Without effective metrics, no reliable way exists to gauge status and manage progress. In addition to its other features and benefits, SystemVerilog provides support for functional coverage. By including coverage in the verification plan from the start of the project and taking advantage of SystemVerilog, the SOC team can employ a complete plan-to-closure methodology that greatly increases the chances for a successful product. EDN

REFERENCE

1 www.systemverilog.org.

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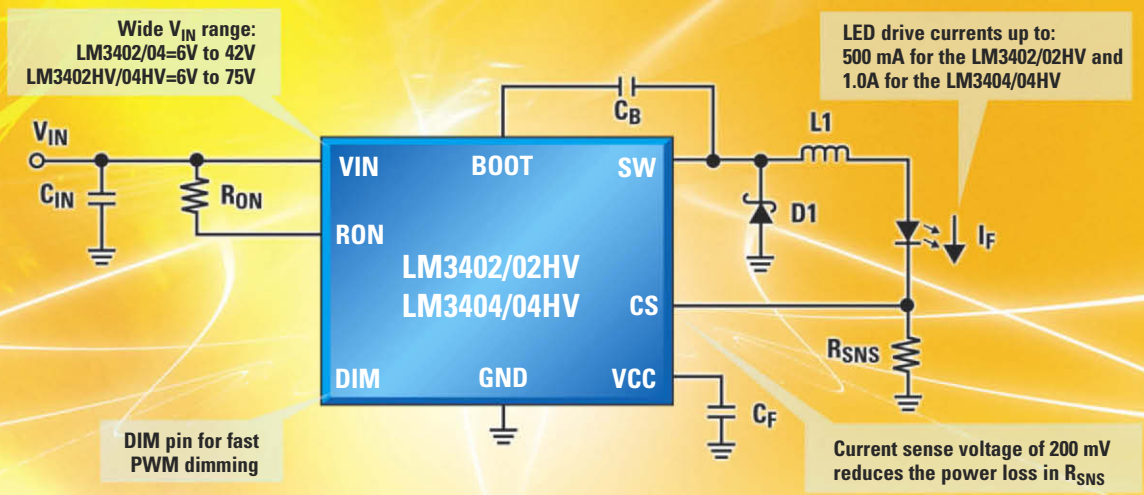

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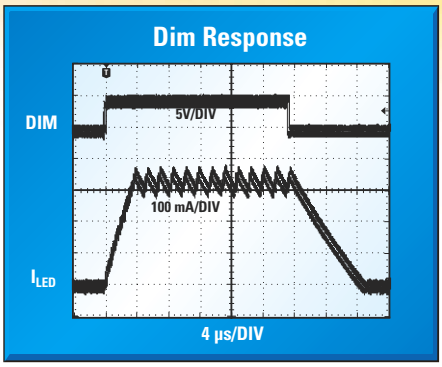

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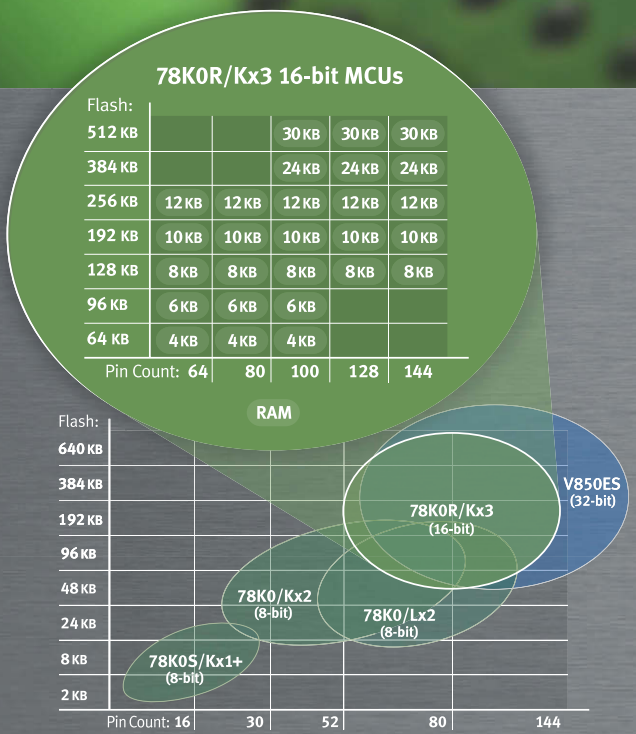

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DESIGN NOTES

36V 2A Buck Regulator Integrates Power Schottky

Design Note 412

David Ng

Introduction

Everyone wants more power in less space. However, the task of designing a power supply is easy to describe but difficult to execute. How does a designer select an optimal set of components that yields the best possible power supply in terms of size, cost and performance? Well, it is easier if the selection is reduced to only a handful of components.

For instance, the LT®3681 reduces parts selection to only a few passive components by integrating all of the power semiconductors necessary to make a buck converter into a single package. Don't think that this high level of integration limits the usefulness of this part. The LT3681 accepts inputs from 3.6V to 34V, provides excellent line and load regulation and dynamic response, and offers a high efficiency solution over a wide load range while keeping the output ripple low during Burst Mode® operation. Furthermore, its frequency is adjustable from 300kHz to 2.8MHz, enabling the use of small, low cost inductors and ceramic capacitors.

A Small, Simple Solution

The LT3681 integrates a wide input voltage range, high performance buck controller, power switch, high side bootstrapping boost diode and a power Schottky diode. All of these attributes are crammed into a tiny but thermally efficient 14-pin 3mm × 4mm DFN package. So, all a designer needs to implement a full-featured buck converter is to add the output LC filter and a few passives.

The most obvious advantage of having the power Schottky diode integrated into the LT3681 is space savings, reducing the amount of board space required by the complete regulator by 15% or more. Moreover, the power Schottky diode has been optimized for the intended operation of the LT3681, so there is no need to agonize over finding the perfect form, fit and function diode for the application. Figure 1 shows a schematic of the LT3681 producing 5V at 2A from an input of 6.3V to 34V and Figure 2 shows the efficiency for a 12V input.

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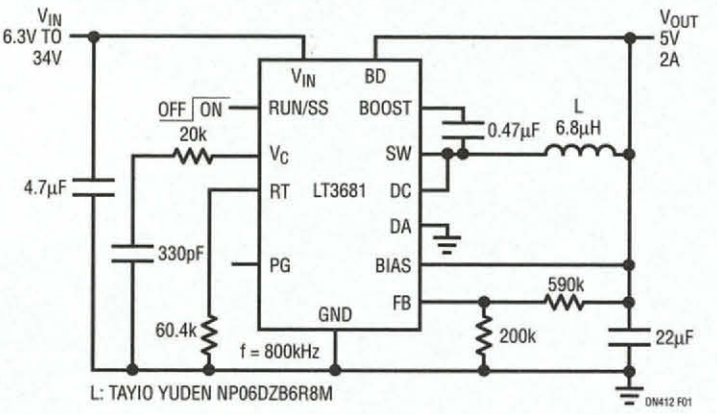

Figure 1. The LT3681 Integrates All of the Power Semiconductors Necessary to Make a Simple 2A Buck Converter

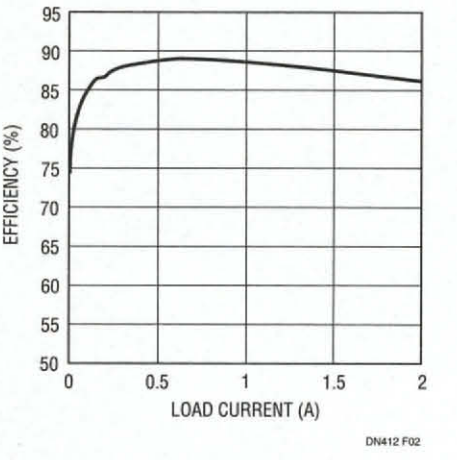

Figure 2. The LT3681 Boasts High Efficiency (12V Input to 5V Output)

Low Ripple and High Efficiency Solution over a Wide Load Range

The LT3681 switching frequency can be programmed from 300kHz to 2.8MHz by using a resistor tied from the RT pin to ground. The LT3681 offers low ripple Burst Mode operation that maintains high efficiency at light loads while keeping the no load output voltage ripple below $15mV_{P-P}$.

During Burst Mode operation, the LT3681 is able to deliver current in as little as one cycle to the output capacitor followed by sleep periods where all of the output power is delivered to the load by the output capacitor. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to only 55µA. As the load current decreases toward no load, the percentage of time that the LT3681 operates in sleep mode increases and the average input current is greatly reduced, so high efficiency is maintained.

Figure 3 shows the low ripple and single cycle burst inductor current at no load for the 3.3V regulator shown in Figures 1 and 2. The LT3681 has a very low shutdown current (less than 1µA), significantly extending battery life in applications that spend long periods in sleep or shutdown mode.

For systems that rely on a well-regulated power source, the LT3681 provides a power good flag that signals when V_{OUT} reaches 90% of the programmed output voltage.

A resistor and capacitor on the RUN/SS pin programs the LT3681's soft-start, reducing the inrush current during start-up. In applications where the circuit is plugged into a live input source through long leads, an electrolytic input capacitor, which has higher ESR than a ceramic capacitor, is recommended to dampen the overshoot voltage. Refer to AN88 for further details.

Frequency Foldback Saves Chips

During short circuit, the LT3681 offers cycle-by-cycle current limit and frequency foldback, which decreases the switching frequency. This increases the off time, reducing the RMS current through the power switch and allowing the inductor current to safely discharge before the next switching cycle begins.

Conclusion

The robust design, small package and high level of integration of the LT3681 make it an excellent choice for a wide variety of step-down applications where a compact footprint and component optimization are critical. The high input voltage rating, high power switch capability and excellent package thermal conductivity adds to its versatility.

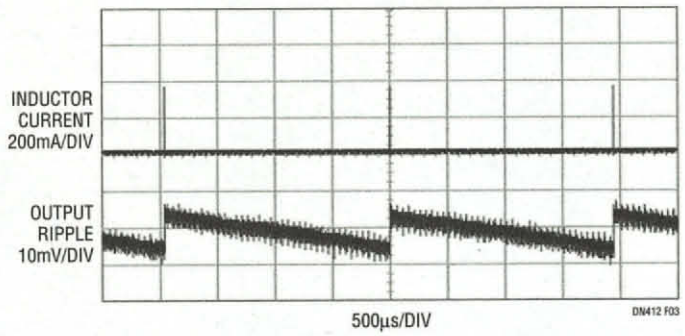

Figure 3. This LT3681 Design Has Only 15mV of Output Ripple, Even at No Load under Burst Mode Operation

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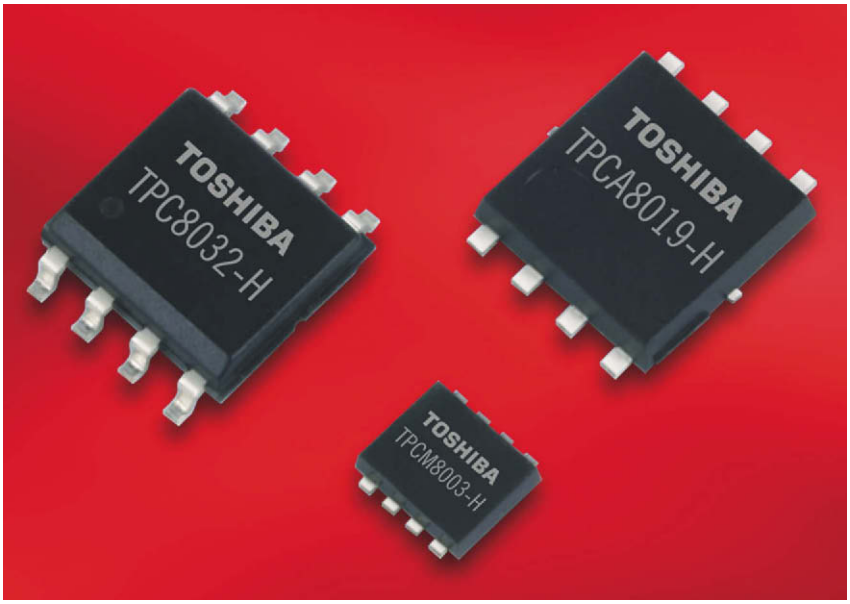

Switching MOSFETs aim at synchronous dc/dc converters

Targeting synchronous dc/dc converters, the UMOS-V high- and low-side switching MOSFETs suit flat-panel displays, servers, desktop PCs, and mobile computers. The low-side MOSFET includes lower on-resistance and a reduced self-turn-on loss using a lower gate-to-drain capacitance and a lower gate resistance. Using a new process technology, the high-side MOSFET enables faster switching using a lower gate charge and a lower gate resistance. Prices for the UMOS-V family range from 60 to 90 cents.

Toshiba America Electronics Components, www.toshiba.com

DirectFET MOSFET suits a range of dc/dc converters

The 150V IRF6643PbF DirectFET MOSFET targets isolated dc/dc converters operating on 36 to 75V universal-input telecom systems and 48V fixed-input systems. A 35A current rating and a 10V on-resistance of 29 mΩ make the device suitable for high-current synchronous-rectifier sockets. The device can also function as a primary-side MOSFET in isolated or intermediate dc-bus converters, providing a 39-nC gate charge and an 11-nC gate-to-drain charge. Available in an SO-8 package, the IRF6643PbF costs $1.24 (10,000).

International Rectifier, www.irf.com

MOSFET reduces switching losses

Joining the vendor's CoolMOS CP series, the CoolMOS CP 500V power MOSFET provides 50V/nsec switching speeds. The device has a 6.7Ω×nC figure of merit (on-state resistance times gate charge), reducing the conduction and switching losses

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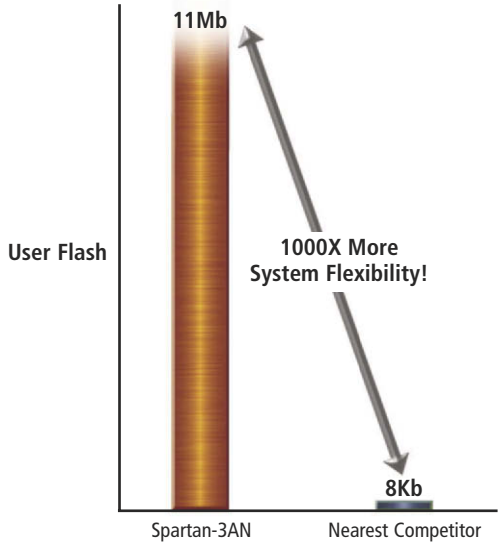

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and increasing the efficiency of power-supply designs. Available in a TO-220 package, the 140-mΩ CoolMOS CP 500V costs $1.35 (1000).

Infineon Technologies, www.infineon.com

Power MOSFETs feature double-sided cooling

Adding to the vendor's PolarPAK power-MOSFET family with double-sided cooling, the n-channel 20, 30, and 40V devices provide a 1.4- to 2.6-mΩ on-resistance range. For applications in which minimizing switching losses is more critical than low-conductance losses, the family includes the 30V SiE830DF and the 40V SiE832DF with a 4.2- and a 5.5-mΩ on-resistance, respectively; both have a 10V gate drive. The PolarPAK power MOSFETs cost $1.50 (100,000).

Vishay Intertechnology, www.vishay.com

Gate drivers switch MOSFET on and off to limit power dissipation

Driving 30A at 1200V in industrial applications, the high-frequency FOD3180 and FOD3181 MOSFET gate drivers provide 200-nsec maximum rise/fall times. The optically isolated devices quickly turn power MOSFETs on and off to limit power dissipation. The FOD3180 has a 2A peak-output current, allowing you to drive MOSFETs without additional amplification. The devices target solar inverters, high-performance UPSs (uninterruptible power supplies), dc/dc converters, and plasma-display panels. Additional features include a 5000V isolation rating that meets many safety-certification standards and an undervoltage lockout that protects the MOSFET by keeping it off until the voltage reaches the enabled state. Available in a DIP-8 package, the 2A FOD3180 and 0.5A FOD3181 cost $1.91 and $1.40, respectively.

Fairchild Semiconductor, www.fairchildsemi.com

SiGe HBT provides 2.4- and 5-GHz performance levels

The high-performance RQG2003 power SiGe (silicon-germanium) HBT (heterojunction bipolar transistor) provides 2.4- and 5-GHz performance. At 5.8 GHz, the SiGe device features a 6.4-dB power gain, a 1-dB gain-compression power of 26.5 dBm, and a 33.6% power addition efficiency. At 2.4 GHz, the device provides a 13-dB power gain, a 1-dB gain-compression power of 26.5 dBm, and a 66% power addition efficiency. Built using an SiGeC process, the RQG2003 costs 87 cents.

Renesas Technology America, www.renesas.com

COMPUTERS AND PERIPHERALS

Storage processor features content security

Providing content security using automatic drive-locking, the SteelVine SiI5733 storage processor also features the previous generation's cascading and multi-RAID (redundant-array-of-inexpensive-disks) modes. The Safe33 and Safe50 multi-RAID modes divide an external drive into virtual-storage areas focusing on data protec-

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tion and increased capacity. Additional features include drive cascading for dynamic capacity expansion, RAID 0, and RAID 1. The device's SATA ports operate at 3 Gbps and comply with the eSATA Generation 2m portions of the SATA 2.5 specifications. The SiI5733 costs $5.

Silicon Image, www.siliconimage.com

Multidisplay device uses digital outputs

Joining the vendor's DualHead-2Go multidisplay devices, the Digital Edition features digital outputs. The device provides a 3840×1200-pixel stretched desktop or dual 1920×1200 pixels across two displays. The device supports Windows Vista, Windows XP, Windows 2000, and Windows XP 64-bit operating systems, as well as Mac OSX. The DualHead2Go Digital Edition costs $229.

Matrox Graphics, www.matrox.com

Graphics card features 320 Mbytes of GDDR3 frame-buffer memory

The XLR8 GeForce 8800 GTS graphics card features 320 Mbytes of high-speed GDDR3 (graphics-double-data-rate 3) frame-buffer memory and a 500-MHz core clock. Outputs include two DVI (digital-video-interface) slots and an HDTV/S-Video slot. The 8800 GTS costs $299.99 and $349.99 from online vendors and retailers, respectively.

PNY Technologies, www.pny.com

Wide-screen LCDs have VGA, DVI-D, and DVI-I inputs

The MultiSync 24-in. LCD2690-WUXi and 26-in. LCD2490-WUXi wide-screen LCDs support 25.5- and 24.1-in. visual displays. The desktop monitors provide VGA, DVI-D, and DVI-I outputs; the DVI-D connector supports HDCP (high-bandwidth digital-content protection). The devices have a 1920×1200-pixel native resolution and a 16-to-10 aspect ratio. The LCD-2690WUXi and LCD2490WUXi cost $1699.99 and $1499.99, respectively.

NEC Display Solutions of America, www.necdisplay.com

Digital-shared-storage device has a 1-Tbyte capacity

Compatible with wired and wireless networks that come with a lighted on/off button, the My Book World Edition II digital-shared-storage appliance features a dual-drive system with a 1-Tbyte capacity. Additional features include an LED that exhibits the remaining storage capacity, easy-to-use backup software, and a three-year limited warranty. The My Book World Edition II costs $499.

Western Digital, www.westerndigital.com

External hard drive comes in 100-, 120-, and 160-Gbyte capacities

Using the vendor's 2.5-in. hard-disk-drive technology, the USB 2.0 portable external hard drive comes in 100-, 120-, and 160-Gbyte capacities. Also functioning with USB 1.1, the devices are compatible with Microsoft Widows 2000, Windows XP, Windows Vista, and the Macintosh OSX 10.3.9. Using NTI Shadow software, the hard-disk drive provides automatic backup once users set the parameters. The portable hard drive measures 3.5×5.6×0.94 in. and costs $139.99.

Toshiba Storage Device Division, www.toshibastorage.com

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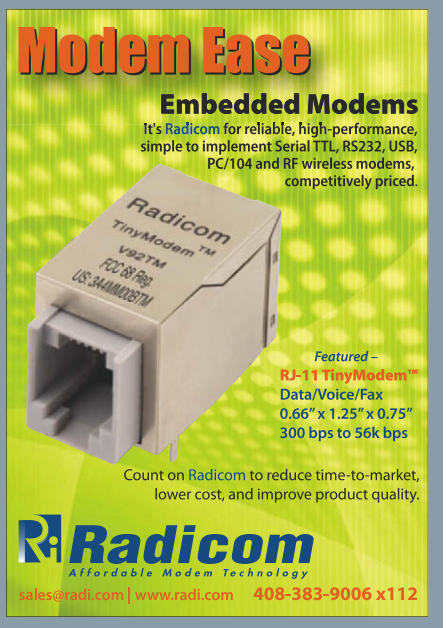

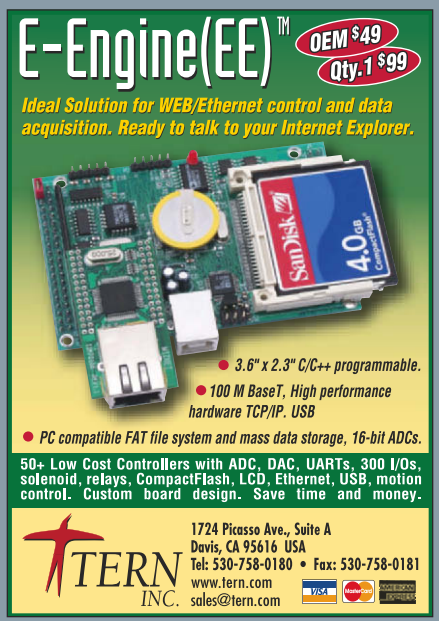

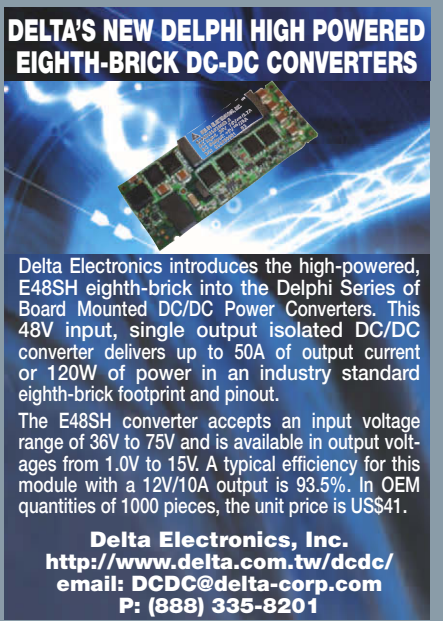

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LOOKING AHEAD

TO THE NAB CONFERENCE

The 2007 NAB (National Association of Broadcasters) Show (http://nabshow.com) opens April 14 in Las Vegas. The show is primarily a way for equipment providers to pitch to broadcasters; however, it has also become the forum in which all the providers of digital-media products look into each other's booths to gauge the state of the industry. Many of the session topics are also informative. There will be training for broadcast engineers on nonconventional themes, such as understanding MPEG-4 and H.264 video encoding; creating a digital-video network within a studio; and learning the art of podcasting.

But perhaps the most startling sign of the times is this year's keynote speaker in the Innovator's Spotlight slot: not an influential broadcaster or a studio chief, but Eric Schmidt, chairman and chief executive officer of Google. Times are changing.

LOOKING BACK

AT THE SEARCH FOR A DECENT BATTERY

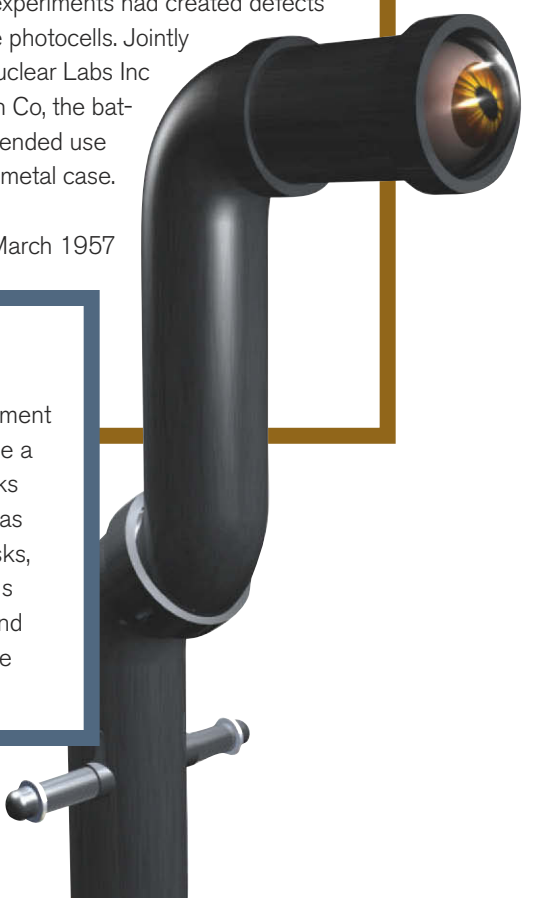
The decay of the beta-emitting radioisotope in an oxide of Promethium 147 has successfully powered a miniature battery about the size of a shirt button. The sandwichlike design employs two-step energy conversion. Beta emissions from the Promethium oxide in the center of the sandwich strike surrounding layers of phosphor, which in turn emit red and infrared light. Two or more photocells at the outside of the sandwich then convert the light into electrical current. The sandwich design protects the photocells from direct exposure to the beta radiation, which in previous experiments had created defects in the crystal structure of the photocells. Jointly developed by Walter Kidd Nuclear Labs Inc and the Elgin National Watch Co, the battery is said to be safe for extended use by humans if it is in a dense metal case.

—*Electrical Design News*, March 1957

LOOKING AROUND

AT MULTICORE ARCHITECTURES

Architects have for years used combinations of processors to implement their designs. But in the past, embedded designs have tended to use a processor-per-task approach, in which the processors and their tasks were only loosely coupled to each other. That situation is changing, as architects turn to multiple cores not just to execute independent tasks, but also to accelerate the execution of a single task. This fact means much tighter coupling between the cores, shared-data structures, and a level of design that engineers currently don't understand. Multicore embedded computing may be the next big frontier for the industry.



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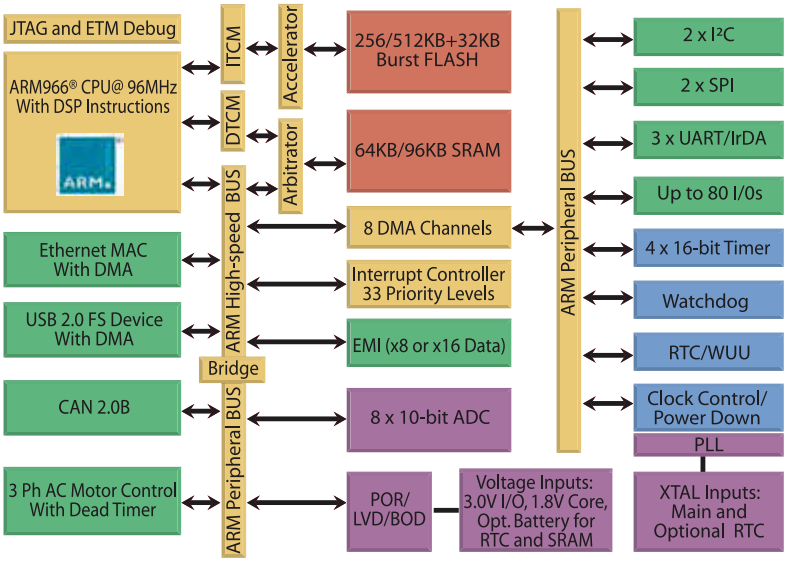

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STR911FM44X	512 + 32	96	8x10-bit				40 (16)	LQFP80		USB, CAN
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